

MODEL

1501A

PROGRAMMABLE
PULSE
GENERATOR

TECHNICAL MANUAL



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INSTRUCTION MANUAL
1501A
PROGRAMMABLE PULSE GENERATOR

Serial No.

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INSTRUMENT WARRANTY

All E-H International, Inc., products are warranted for a period of one year from date of delivery. These products are warranted to be free from defects in material and workmanship, suitable for normal use and service under normal conditions, and able to meet any applicable specifications accepted in writing by E-H International, Inc. No claim under the warranty will be accepted unless it is made in writing to E-H International, Inc., immediately after discovery of defect or in any case, within one year of delivery. No other warranty, express or implied exists outside this warranty. E-H International, Inc., is not liable for any commercial losses or other consequential damages incurred or sustained as a result of any defective or nonconforming product. E-H International's obligation with respect to losses is limited, under this warranty, at E-H International's option, either to the replacement (by delivery F.O.B. Oakland, California) or repair of its manufactured products which prove to be defective or nonconforming. This warranty does not apply to any products improperly applied or used or which have been subjected to intentional or negligent misuse or accident, or which have been in any way modified by others without the express written agreement of E-H International, Inc. Any product claimed to be defective during the warranty period must be returned to an authorized E-H International, Inc., repair center, with transportation charges prepaid. The product will be repaired and returned to the purchaser with return transportation prepaid by E-H International, Inc. If no defect in the product is found, or if failure is due to misuse or accident, such product will be returned to the purchaser with repair and transportation charges billed collect.

For in-warranty repair of this instrument, contact E-H International, Inc., Customer Service Department and provide the following information:

- (a) Instrument model number and serial number.
- (b) Details concerning the nature of the malfunction.

Shipping instructions, or repair information and parts will be sent to you promptly.

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SECTION 1

SPECIFICATIONS

1-1 GENERAL INFORMATION

The E-H Model 1501A Programmable Pulse Generator (called Model 1501A hereafter) is a compact unit, designed to meet the requirements for a fully programmable pulse generator in high-speed, automatic test system applications. Programmable 10 V output amplitude, and 50 MHz repetition frequency capabilities make the Model 1501A an ideal choice for any application requiring TTL and DTL drive sources.

Full control of all pulse parameters is provided by external programming lines. Interface to integrated circuits and adaptation to current logic levels is enhanced by the addition of variable baseline offset and polarity inversion functions, which allow simulation of positive, negative or inverted logic. Baseline offset is inserted after the attenuator to permit full use of the offset capability.

Synchronous and asynchronous gating are provided as useful features for systems applications. Distortion is less than 5% peak-to-peak for all functions.

Normal/inverted and single/double pulse modes are built into the Model 1501A. In the inverted mode an extremely high duty cycle can be achieved for the output pulse.

1-2 SPECIFICATIONS (All specifications assume a 50 ohm resistive load on the output. See also Subsection 1-4, Accuracy.)

a. Pulse Repetition Frequency

From 0.5 Hz to 50 MHz in 8 decade ranges

b. Pulse Delay

From 10 ns to 1 s in 8 decade ranges

c. Pulse Width

From 10 ns to 1 s in 8 decade ranges

d. Jitter

Less than 0.1% of setting +50 ps; applies to frequency, delay, or width jitter.

e. Duty Factor

Greater than 50%; applies to either delay or width circuit.

f. Modes

Normal/Inverted and Single/Double Pulse

The inverted mode allows an extremely high duty cycle for the output pulse.

g. External Drive

Input drive signal must go from less than 0.75 V to greater than 1.5 V into a 300 ohm load. Maximum input 5 V. Maximum frequency 50 MHz.

h. Synchronous Gate

Input drive signal must go from less than 0.75 V to greater than 1.5 V into 375 ohm load. Both gate on and gate off modes are under program control.

i. Asynchronous Gate

Input drive signal must go from less than 0.75 V to greater than 2.5 V into a 50 ohm load. Gate off operation only.

j. Trigger Output

Greater than +1.5 V into 50 ohms; greater than +3 V into high impedance. Width 10 to 100 ns depending on frequency. Two additional clock outputs available for master/slave pulse generator operation. Output levels same as trigger output. Clock outputs are nominally 25-30 ns early with respect to trigger output.

k. Minimum Double Pulse Spacing

Less than 12% of width range maximum

l. Amplitude

+3 V to +10 V into 50 ohms from a 50-ohm source; attenuator accuracy is $\pm 2\%$.

m. Offset

0 to +5 V (+50 mV) into 50 ohms independent of attenuator setting. The maximum output amplitude is restricted to +10 V for the sum of the pulse and offset amplitudes when driving a 50 ohms load. in the off position offset is less than ± 10 mV.

n. Pulse Distortion

Less than 5% peak-to-peak for all amplitudes and for all rise and fall times greater than 3 ns.

o. Rise and Fall Time

Less than 3 ns to 0.8 ms in 6 decade ranges; separate rise and fall verniers

p. Ramp Linearity

Less than $\pm 1.5\%$ above 100 ns; less than $\pm 5\%$ 10 to 100 ns.

1-3 ACCURACY (including all programming options)

a. Repeatability

$\pm 1\%$ of setting

b. Programming Error

$\pm 5\%$ of desired value for amplitude, frequency and Offset, $\pm 5\%$ ± 3 ns for rise and fall times, delay and width, except $\pm 15\%$ of value for 10 ms - 100 ms and 100 ms - 1 s ranges. Delay and width relate to fastest ramps.

NOTE: Programming accuracy specs refer to 10% to 99.9% of selected full scale range only. Programming below 10% of selected range is non-linear.

c. Setting Time

Less than 2.5 ms for attenuation and polarity; less than 750 μ s when going to or from ramp ranges 0 and 1.

1-4 MISCELLANEOUS

a. Dimensions

5-1/4 in. (13.3 cm) high, 19 in. (48.2 cm) wide, 20-3/4 in. (52.7 cm) deep

b. Weight

35 lbs. (15.9 kg)

c. Power Requirements

100, 117, or 230 VAC $\pm 10\%$; 50-60 Hz, approximately 200 VA.

d. Operating Temperature Range

0°C to +55°C

e. Temperature Coefficient of Pulse Parameters

Frequency	+0.3%/degree C.
Width and Delay	+0.1%/degree C.
Amplitude	+0.05%/degree C.
Offset	+0.05%/degree C.

SECTION 2

OPERATING INFORMATION

2-1 GENERAL INFORMATION

This section of the Instruction Manual gives installation procedures, and describes the operating controls and modes of operation.

The Performance Verification Procedure given in Section 4 of this manual serves as a receiving inspection. All of the operating controls are shown on the Block Diagram in Section 3 in relation to the functional elements of the instrument. Specifications from Section 1 which directly affect operation of the instrument are reiterated in this section.

2-2 INITIAL INSPECTION AND INSTALLATION

a. Unpacking

Unpack the instrument and verify that it is intact and as ordered. Inspect the instrument for any physical damage. If damage of any sort is found, a claim should be filed immediately with the carrier. As soon as possible, the instrument should be given a thorough electrical inspection. The Performance Verification Procedure given in Section 4 is recommended for this purpose. If the instrument fails to operate properly or does not meet specifications, contact an E-H Representative.

NOTE

Unauthorized repair or parts replacement during the warranty period may void the warranty. The warranty and instruction for in-warranty repair of this instrument are given on Page i of this manual, opposite the Table of Contents.

b. Installation

The E-H Model 1501A is supplied in a rack-mount configuration. Refer to Figure 2-1 for mounting dimensions. Power connection and fuse requirements are silk-screened on the rear panel. Input ac power is connected via the three-conductor power cord (supplied) to rear panel connector J101. The POWER

switch should be turned OFF prior to plugging in the instrument. The instrument is cooled by an internal fan that operates when the POWER switch is turned ON. The top and bottom covers should remain in place when the instrument is in use to provide proper flow of cooling air.

2-3 DESCRIPTION OF CONTROLS AND CONNECTORS

a. Front Panel Controls

Front panel digiswitch programming controls are available as Option 02 (see Appendix C).

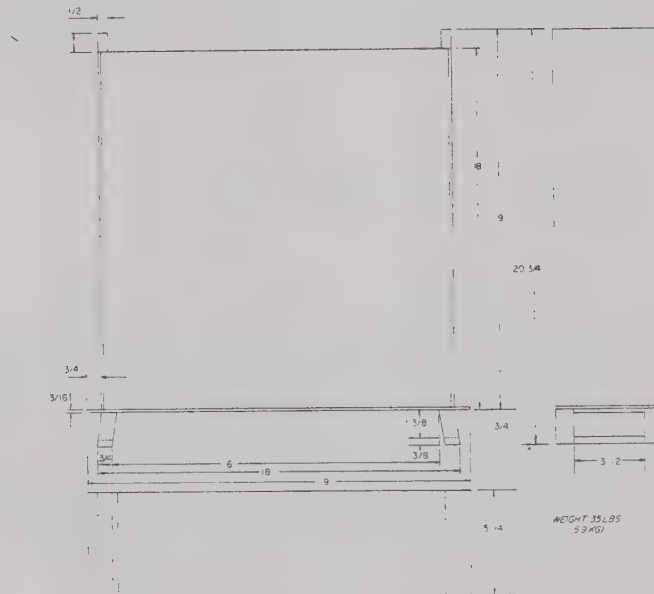


Figure 2-1 Outline & Mounting Dimensions

b. Rear Panel Connectors (Refer to Figure 2-2)

(1) Trigger Output

Greater than +5 V into 50 ohms; greater than +3 V into high impedance. Width 10 to 100 ns depending on frequency.

(2) Clock Outputs

Two additional clock outputs are available for master/slave pulse generator operation. Output levels same as trigger output. Clock outputs are nominally 25-30 ns early with respect to trigger output.

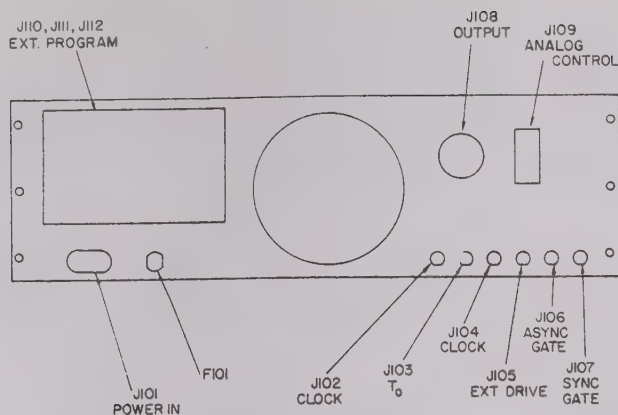


Figure 2-2 Rear Panel Connectors

(3) External Drive Connector

The input drive signal must go from less than 0.75 V to greater than 1.5 V into a 300-ohm load. Maximum input 5 V. Maximum frequency 50 MHz.

(4) Asynchronous Gate In

The input drive signal must go from less than 0.75 V to greater than 2.5 V into a 50 ohm load. Gate off operation only.

(5) Synchronous Gate In

The input drive signal must go from less than 0.75 V to greater than 1.5 V into a 375-ohm load. Both gate on and gate off modes are under program control.

(6) Pulse Output

+39 mV to +10 V into 50 ohms from a 50-ohm source

2-4 OPERATING NOTES

The risetime of the Model 1501A output pulse has appreciable frequency components up to 500 MHz. If any of the connectors, cables, or attenuators used do not have flat responses in excess of 500 MHz, degradation of pulse risetime will result. Mismatch effects can also degrade the pulse shape. When possible, terminate the output of the 1501A into a 50-ohm pure-resistive load. If the input impedance of the device or system under test is other than 50 ohms, use an impedance matching device to minimize the mismatch effects.

(1) Open Circuit Operation

The maximum output amplitude shall be greater than ± 19.5 V peak-to-peak as measured into a load resistance ≥ 5 K ohms. The maximum absolute voltage level from ground shall be limited to 14 V at minimum offset. 1.5 times the offset voltage is subtracted from the 14 V limit for offsets of the same sign as the output pulse, and the value of the offset is added to the 14 V limit for offset of opposite polarity.

2-5 BRIEF DESCRIPTION OF MODEL 1501A OPERATING MODES

a. Ext. Clock

Activating this mode disables the internal frequency circuits (clock) and enables an external trigger signal applied to J105 to control the Model 1501A pulse output frequency from 0 to 50 MHz. Trigger signal is generated for each input to J105 and is available at the normal trigger output connector J103.

b. Db1. Pulse

Activating this function allows pulse pair operation. The first pulse is roughly coincident with the trigger output - the second pulse is spaced by using the DELAY programming. This mode is usable with either internal or external clock.

c. Normal Pulse

Activating this function gives a pulse whose baseline is at the OFFSET level programmed and whose pulsetop is at the AMPLITUDE level programmed (see below).

d. Gate On

Activating this mode allows a signal (or DC level) connected to J107 to gate on the Model 1501A output. In this mode, both internal clock and output circuits are disabled until gated on. When line is ungrounded (high level), gate off signal applied to either Asynchronous or Synchronous gate inputs turns off output. In Asynchronous mode, internal clock runs and trigger signals are generated. When gate signal goes low in Asynchronous mode, first output pulse occurs at next clock period.

e. Pos. Polarity

When this mode is programmed, the leading edge of the pulse moves in a positive direction in normal mode; when the line is ungrounded, the leading edge of the pulse moves in a negative direction in normal mode.

f. +Offset and -Offset

These modes control whether baseline offset is positive with respect to ground or negative with respect to ground.

2-6 234 VOLT OPERATION

a. General

The Model 1501A power transformer primarily is normally connected for 117 V service. For use with 234 V service, the primary must be reconnected. This is accomplished by altering the input connections and jumpers on the ac input terminal strip, TS101. Proper connections for either type of service are shown on the Primary AC Power schematic in Section 6.

b. Reconnection Procedure

- (1) Check the rear panel "Power Data" chart to determine the existing power connections.
- (2) Disconnect the power cord and remove the bottom cover using the procedure given in Subsection 4-4.
- (3) Locate TS101 on the bottom chassis layout drawing in Section 6.
- (4) Remove the terminal strip cover and position the jumpers as shown on the power supply schematic, for the type of service desired.
- (5) Replace the bottom cover on the instrument. Note the change in power connection on the rear panel "Power Data" chart. Change the line fuse, F101, to correspond with the power connection.

2-7 REAR PANEL CONNECTORS

The following is a summary of the input and output connectors located on the rear panel of the Model 1501A.

J101	AC Primary Power Input
J102	Clock Output
J103	Trigger (T_O) Output
J104	Clock Output
J105	External Drive Input
J106	Asynchronous Gate Input
J107	Synchronous Gate Input
J108	Pulse Output
J109	Not Used
J110/111/112/113	Programming Input/Output

See timing diagrams, Figure 2-3 for time relationships.

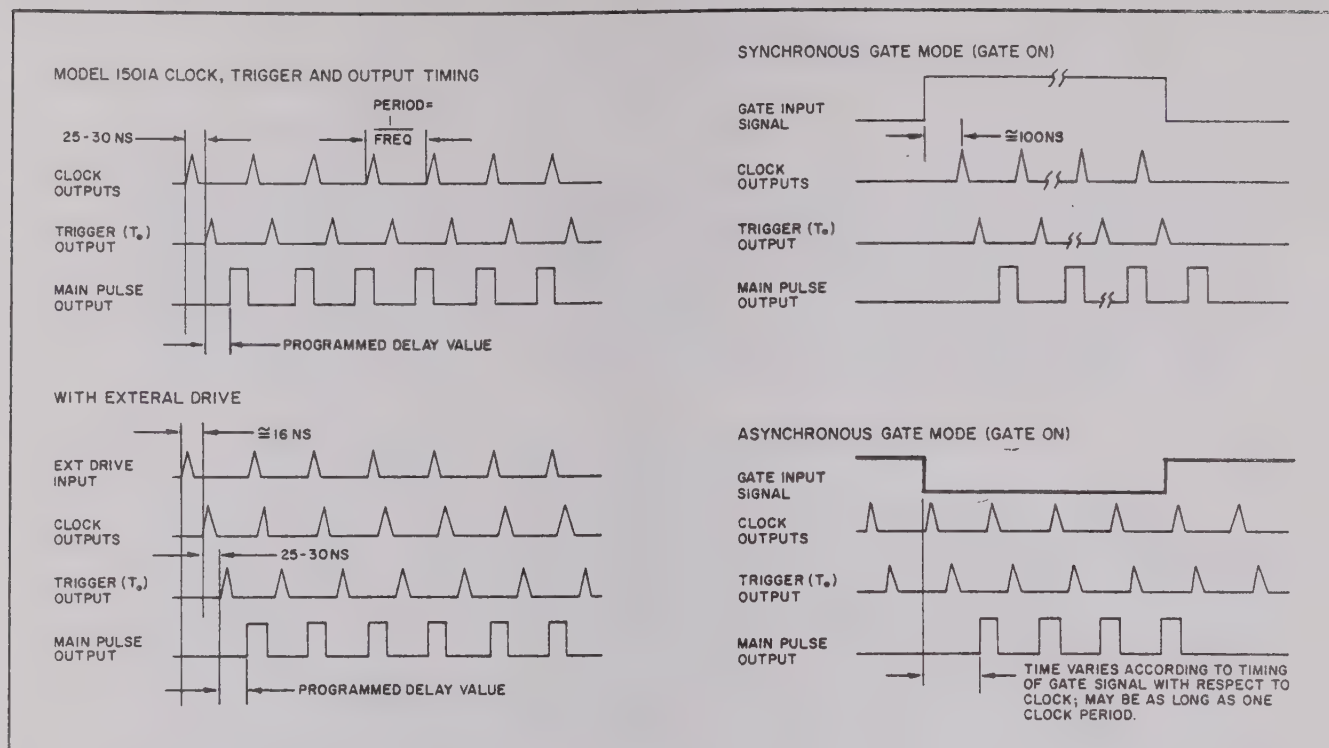


Figure 2-3 Timing Diagrams

SECTION 3

THEORY OF OPERATION

3-1 GENERAL INFORMATION

The following section of this manual contains an electrical description of each of the circuits of the E-H Model 1501A Programmable Pulse Generator. The description is divided into two parts. The first part is a discussion of the block diagram for the instrument, and the second part is a detailed discussion of each of the circuits which comprise this instrument.

3-2 BLOCK DIAGRAM (Refer to Figure 3-1)

The E-H Model 1501A Pulse Generator is basically identical to any conventional laboratory pulse generator with the addition of appropriate programming circuits. The clock multivibrator determines the base repetition frequency range of 5 to 50 MHz. The actual operating frequency is determined by the signal which is supplied by the digital-to-analog converter. All of the remaining clock ranges are generated by dividing the 5 to 50 MHz frequency range by an appropriate value in the divide by 10^n counter. For example, the 0.5 Hz to 5 Hz range is obtained by dividing the basic clock frequency range by 10^7 . The output of the divider is supplied to the input of a buffer amplifier to drive the width and delay circuits and to a trigger driving amplifier which supplies the trigger output pulse from the Model 1501A.

Also associated with the basic clock multivibrator is the synchronous gating circuitry. These circuits provide for synchronously gating the clock on or gating the clock off from a positive going gate signal selected by program control. In cases where external drive is preferred, program control can substitute the output of the external input circuit for the clock circuit.

A second gating circuit is supplied at the input of the delay and width module. This gate is of the asynchronous type.

The delay one-shot operates in decade ranges from 10 nano-seconds to 1 second. The absolute delay within any given range is determined by the setting of the D to A converter. The ranges are determined by the data supplied to the buffer card whose output causes an appropriate range capacitor and charging current to be selected for each of the six ranges. The delay one-shot's output drives, through a set of gates, the width one-shot which has identical ranges and operates in the same manner as the delay one-shot.

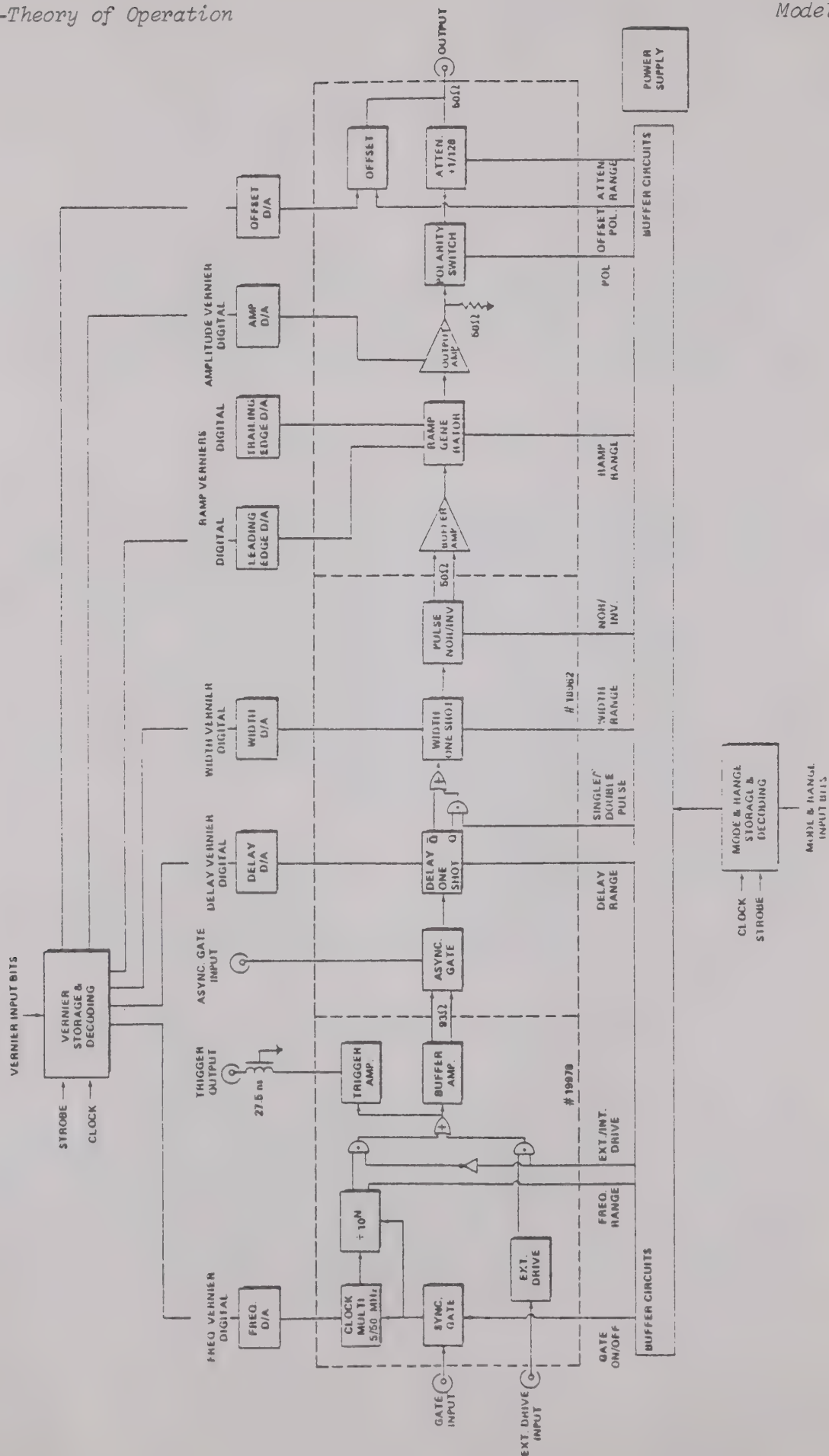


Figure 3-1 1501A Block Diagram

These gates provide for double pulse operation by supplying both the normal and inverted output of the delay multivibrator to the input of the width multivibrator. This causes the width one-shot to trigger on both the leading and trailing edges of the delay one-shot. The output of the width one-shot is amplified and/or inverted by the pulse logic circuit under program control. When the output pulse is to be complemented, the circuit simply inverts the output of the width one-shot providing the appropriate drive form for the output. In the output module the signal is first shaped and amplified and then presented to the input of the ramp generator.

The ramp generator provides five calibrated and one uncalibrated ranges of ramp speed. Each range controls both the leading and trailing ramp rate. However, there are individual D to A cards for the leading and trailing edges of the ramp signal. The output of the ramp drives a quasi-linear amplifier that supplies the needed amplification and also provides the necessary amplitude control. This amplifier drives the junction of a polarity switch and the back match.

The polarity switch consists of a balun and relay combination which drives the output attenuator. This, in turn, supplies attenuation values from unity transfer through an attenuation ratio of 128 to 1, in binary steps under program control. At the output of the attenuator the offset signal, which is derived from the setting of the D to A converter card, is combined with the pulse generator's output in a current summing technique. The resulting output pulse is supplied to the rear panel of the Model 1501A as the output signal.

3-3 CIRCUIT DESCRIPTION

a. General

Each of the functional blocks of the block diagram is described in detail in the following paragraphs. The following definitions are utilized in this direction.

(1) Vernier Input

A vernier input is a 12 bit BCD word converted to a voltage in the range of 0 to 5 V. All vernier inputs are directly proportional to the parameter they control.

(2) Range Input

The range input consists of three digital control lines which are programmed in octal fashion.

(3) Functional Input

A functional input is a single binary line that controls such parameters as positive or negative output pulse, single or double pulse mode, etc.

(4) Logical 1

A logical 1 is the signal level between 0 and 0.5 V.

(5) Logical 0

A logical 0 is a signal level between 2.5 and 5 V.

b. Type B Clock Module

This basic clock multivibrator is composed of transistors Q4 and Q5 and their associated circuitry. This multivibrator is of the conventional emitter coupled form whose collector resistor has been replaced by clamping diodes CR21 and CR22, CR23 and CR24 and current source transistors Q23 and Q24. The charging current for the timing capacitor C4 is supplied by the current source, Q2 and Q3. These transistors are programmed through an input buffer amplifier with transistors Q11 through Q13 providing the vernier control of the clock frequency. Since the charging current of C4 relates directly to frequency, this clock programs frequency directly. The current supplied to the timing capacitor has approximately a 10 to 1 variation from roughly 2 or 2-1/2 mA to 20 or 25 mA. In order to cover this range and maintain proper circuit action, the current sources in the collector of the multivibrator must track the timing current sources. This is accomplished via transistor Q1 which through emitter follower Q25, drives the collector current sources, which supply the appropriate bias currents to the collector of the multivibrator, transistors Q4 and Q5.

Diodes CR21 and CR24 clamp the collectors to a maximum negative excursion of approximately 400 millivolts while diodes CR22 and CR23 provide a positive clamp that is roughly +600 millivolts, thus allowing a 1 Volt collector swing on the clock multivibrator. The reference voltage supply for this

positive clamp is controlled by potentiometer R68 which functions as an overall range adjusting potentiometer. Transistor Q26 shifts the bias point of the voltage source for diodes CR22 and CR23 to compensate for the changes in the clamp diodes due to changing operating points. The magnitude of this correction is controlled by potentiometer R53. Potentiometer R26 provides compensation for general circuit non-linearities that occur near the low frequency end of the vernier range.

The output of the clock, which is taken from buffer transistors Q9 and Q10, drives the countdown amplifier Q14, Q15 and Q18 and the busdriver Q19 and Q30. The output of the count down amplifier drives a series of decade counters (ICs 1 through 7) which divide the basic clock frequency by any power of 10 from 0 through 7. The operation of this circuit can be described by a simple example. Assume that we wish to be in the frequency range of 50 to 500 kilohertz. Hence, we wish to divide the basic clock frequency by 100. To do this the range input is decoded by IC8 (a one of 8 decoder) to produce a logical 1 on pin 12 and logical zeros on all other outputs. The logical 0 high level at pin 10 provides a logical 0 at pin 12 of IC12. This allows the first decade to run. The logical 0 at the output of IC12 pin 12 and the logical 0 from pin 11 of the IC8 produce a logical 1 state at pin 11 of IC11 which permits the second decade to count (these two decades require opposite preset signals). The logical 1 at pin 11 of IC11 provides a logical 0 at pin 8. The logical 1 from pin 12 of IC8 forces pin 3 of IC11 to go to the logical 0 state. This in turn presets IC5. The 0 state at this point provides a logical 0 at its output which presets IC4 to the count of 9. This action propagates down the chain presetting counters 3, 2 and 1 to the count of 9. Whenever IC6 reaches the count of 9, the bus connected to the base of transistor Q20 moves positive supplying the logical 0 to pin 11 of IC12. When IC7 reaches the count of 9, lines 9 and 10 go to a logical 0 state which provides a logical 0 from pin 8 of IC12. This output pulse, which is 1 clock cycle long, is supplied to the bus driving amplifier, Q35 and Q36. Since we are in fact counting down, current switch transistor Q37 is turned on and transistor Q38 is turned off, as is transistor Q40. So the only amplifier on the bus is the one driven from the countdown. This in turn supplies the signal for the output of the board via transistors Q45 and Q46 and to the external trigger amplifier, Q41, Q42, Q47, Q48, Q49, Q50 and Q51.

The board's output amplifier drives twin 93 ohm coaxial cables in a differential mode to supply drive to the input of the width and delay module. The trigger output amplifiers consists of two current mode amplifier stages and emitter followers Q49, Q50 and Q51 which are intended to drive 50-ohm loads. However, these circuits are series backmatched and will drive nearly any external impedance. When a gating signal is applied to the internal clock, a positive level is supplied to the base of transistor Q19 via the protective diode bridge, CR1 through CR4. Q19 functions as a buffer stage to drive IC13 and IC14 which function to provide inversion of the in-put signal under the control of the gate ON/OFF functional input. In the gate OFF mode, the output of IC13, pin 6, is at a logical 0 state. This condition allows the decade divider to operate and bias transistor Q21 while cutting off transistor Q22. In this condition the base of transistor Q6 will be biased one diode drop positive with respect to the bias voltage of transistors Q2 and Q3, hence transistor Q6 will not conduct. When a positive signal is applied to the gate input, transistor Q21 is turned off, Q22 turns on, biasing Q6 to a voltage one diode drop negative with respect to the base of Q3. This in turn robs emitter current from transistor Q3 and conducts it to ground via the collector of Q6. This disables the clock and places it in a condition ready to start the next cycle.

The applied gating signal also causes the preset counter (via a logical 1 at pin 2 of IC12) to preset the decade divider to a count of 899999 so that the first clock pulse will cause IC7 to produce an output signal and hence to produce the appropriate drive for the width and delay board in response to the removal of the gate OFF signal. Of course if the functional control line is in the gate ON mode, exactly the opposite operation occurs. That is, the clock is normally disabled and the counter is normally preset to 899999, and when a positive signal is applied to the gating input, the clock turns on and a count down goes into normal operation.

The external drive signal is applied to transistors Q31 and Q32 through the protective diode bridge CR25, CR26, CR27 and CR28 and coupling zener CR29A. These transistors form a Schmitt trigger that shapes the input signal and drives the bus amplifier Q33 and Q34. In the external mode, current is supplied to the emitters of transistors Q33 and Q34 via transistor Q40 while transistors Q38 and Q37 are disabled.

c. Width and Delay Module

The input signal to the width and delay module is supplied to the bases of current mode gating stage Q22, Q23 and Q24 via zener diodes CR4A and CR4B. When a gating signal is applied to the gate input, the flip-flop which is made up of two of the gates of IC3, toggles on the clock pulse to provide a coherent gate signal to the gating transistor Q24. Q24 is biased to remove current from the emitters of Q22 and Q23 and disables the stage. When the gate signal returns to ground, Q24 is returned to a normal high state and cuts off. The current is then rerouted to the current mode amplifier, Q22 and Q23. The collector of Q23 drives an active clipping line (Q58, L4, R71 and R75) which produces a 5 nanosecond positive pulse and a one volt pedestal. CR6 and CR7 isolate the base of Q25 from the 1 V pedestal but pass the 5 nanosecond trigger pulse.

The delay one-shot consists of transistors Q25, Q26 and Q27 and their associated circuitry. This multivibrator operates in the following fashion. Normally transistors Q27 and Q26 are on and transistor Q25 is off. The collector potential of Q27 is determined by the negative clamp diode, CR3. When the gating amplifier provides a trigger pulse to the one-shot, transistor Q25 turns on and Q26 and Q27 are turned off. The collector potential of Q27 then rises to the positive clamp potential set by CR2.

The emitter of transistor Q26 is provided with a capacitance to ground and with a positive current source. This current source charges the emitter capacitor of this transistor in a positive direction until transistor Q26 begins to turn on. This action again turns transistor Q27 on and regeneratively drives transistor Q26 so that the timing capacitor in the emitter of Q26 is discharged rapidly through clamping diode CR13. Once the timing capacitor is discharged the one-shot is back in its quiescent condition ready to be triggered again.

The delay vernier control provides the reference voltage for positive clamp CR2 via the transistor buffer amplifier chain Q17, Q18 and Q19. Varying this bias voltage to the positive clamp diode determines the change in voltage of the timing capacitors and hence the period of the one-shot. Since we are programming the change in voltage to a capacitor, we are in effect directly controlling the period of the one-shot. The 8 ranges of this one-shot are provided by capacitors C8, C25, C26, C27, and C42 and by varying the charging current to the timing capacitors as supplied by the current source transistor Q6.

The ranging circuit operates in the following manner. A range input is supplied to the 1 of 8 decoder, IC2, which in turn activates the transistor switches to turn on the appropriate timing capacitors and controls the current source for the timing capacitors. In the shortest delay range, none of the programmable timing capacitors are activated. Hence, C8 is the only timing capacitor in the circuit while transistor Q7 is saturated. Approximately 10 milliamps of charging current is available to the timing capacitor during this time. In the next lower range, 100 nanoseconds to 1 microsecond, pin 2 of IC2 goes to a logical 1 state which turns on transistors Q57 and Q55 and switching transistor Q56, which connects the timing capacitor, C27, to ground. On the next range down pin 2 goes to a logical 0 and pin 3 becomes a logical 1. This in turn saturates switching transistor Q42 which connects timing capacitor, C25, to ground. In the 10 microsecond to 100 microsecond range, the next range down, pin 4 becomes a logical 1 with all other pins at logical 0, which again activates switching transistor Q42, thus connecting capacitor C25 to ground and also supplies a logic 1 to the input of IC1 producing a logic 0 at the output pin 3 of IC1. This high logic level causes transistor Q7 to be cut off reducing the timing current by a factor of 10. Transistor Q28 is also cut off, reducing the bias current to the one-shot. This causes an approximate decade step in the time required to charge capacitor C25. The error term generated is due to the change in bias current to the timing transistor. This is corrected by the current supply to R137, and to the base of transistor Q20, the bias source for the negative clamp. The 100 microsecond to 1 millisecond range is generated when the input causes pin 13 to become a logical 1. With this input low, timing capacitor C26 is activated, and the charging current to the timing capacitor by a factor of 10 while maintaining capacitor C26 active in the circuit. On the 10 ms - 100 ms range C42 is activated and the charging current is 10 milliamps. On the 100 ms - 1 s range, the charging current is reduced by a factor of ten.

(1) Delay Buffer Amplifier

The output of the delay one-shot is coupled via NPN current mode pair Q29 and Q30 to the bases of the current mode pair, Q31 and Q32, whose collectors drive active clipping lines. Q31 collector drives Q59, L5, R47 and R48 only in the Double Pulse Mode and provides a start of delay trigger to the width one-shot. In Single Pulse Mode, Q60 shunts all

of Q31 collector current to prevent the start of delay trigger. Q32 collector and Q61, L6, R149 and R150 produce an end of delay trigger to the width one-shot.

(2) Width One-Shot

The width one-shot consists of transistors Q33, Q34, Q35, and their associated circuitry. This circuit operates in exactly the same fashion as does the delay one-shot and will not be discussed in any further detail.

The output of the width one-shot drives current mode pair Q38 and Q39. As a function of the normal/inverted control line (pin C7) either transistor Q36 or Q37 is saturated. The saturated transistor shorts the current mode pair collector to the +5 V supply eliminating the output signal from this source. The other transistor is cut off and allows the signal from its collector to be coupled to the base of the output buffer Q40 and Q41. This signal is amplified by the buffer stage and drives a balanced 50-ohm transmission line system to the output board. When the normal/inverted line is placed in the opposite state, the opposite collector of the current mode pair, Q38 and Q39, is connected to the base of the output drive pair.

d. Type C Output Board

The input signal for the output board is applied through isolation transformer T1 to the dc restoring flip-flop, Q7 and Q8, through differentiating capacitor, C1. This circuit provides isolation of the output circuit from the timing circuits. The output of the restoring flip-flop drives a two stage current mode amplifier, Q50 and Q51, and Q18 and Q19. This amplifier in turn drives the current switching bridge which consists of transistors Q55 and Q56 for the current source side and transistors Q57 and Q58 for the current sink side. In the final analysis this entire circuitry simply determines whether current source Q11 and Q12 or current sink Q53 and Q54 are connected to the input side of R66. The output of this resistor, R66, provides either a constant current source or a constant current sink for the timing capacitors. The constant current charging and discharging of these timing capacitors provides the necessary linear ramps for the output amplifier section. The input of this amplifier is transistor Q27 which is an emitter follower driving a current mode pair consisting of driver

transistors Q28, Q59 and Q60 and output transistors Q37 and Q62. The input transistors are operated in parallel as are the two output transistors. The output of this amplifier is coupled via a polarity switching relay and a balun to the input of a pi network attenuator system. The first section of the attenuator is a divide by two network which is either enabled or disabled by relay K2. The second section is a divide by four attenuator which is controlled by relay K3. The final section, a divide by 16 attenuator, is controlled by K4. The output of this attenuator section is coupled directly to the output of the instrument. Also connected to the output of the attenuator is the offset circuit which provides an offset current to the output which is independent of the setting of the attenuator. The output amplifier also drives a 65-ohm resistor and other miscellaneous networks whose cumulative effect is to provide a 50-ohm source impedance for the pulse generator. This source impedance, of course, is provided to minimize the effect of cable reflections and mismatched loads. To illustrate this operation a positive, normal pulse's path will be outlined. When the pulse starts transistor Q7 is turned off. This results in the current sink, Q54, and Q55, being connected via transistor Q58 to the timing capacitor which has been selected. Before the pulse had occurred diode CR30 had clamped the timing capacitor and the emitter follower's base to a potential slightly positive of the -20 V levels. This action completely cuts off the output pair, transistors Q62 and Q37. As the timing capacitor starts to discharge the voltage on the emitter of Q27 moves in a negative direction which allows current to be switched from the driver, transistors Q28, Q59, and Q60, to the output pair and hence on to the polarity control relay. This transfer of current to the output continues until the clamping diode, CR31, catches the bases of the output driver transistors. Shortly after this occurs clamping diode CR29 catches the ramp timing capacitor and also prevents it from continuing in a negative direction. It should be pointed out that the current from current source transistor Q83 in the emitter circuit of the output amplifier is always sufficient to provide some on current for the driver transistors. The output of this amplifier is now coupled through the polarity switch which then selects the direction of input to the balun so that the pulse will be inverted before going to the attenuator. At the end of the pulse the input restoring flip-flop changes state and causes a current source, Q11 and Q12, to be coupled to the timing capacitor instead of the current sink via transistor Q56. This current now charges the timing capacitor in a positive direction. As soon as the timing capacitor has moved sufficiently far so that the emitter follower again

starts to draw current, the current in the output pair begins to reduce. This current reduces to zero before the clamping diode, CR30, clamps the positive charging of the timing capacitor. The circuit is now ready to produce the next output pulse when again the restoring flip-flop changes state. The ramp timing capacitors are selected via the three data bits supplied to pins A1, A2, and A3. These signals are coupled via isolating transistors Q68, Q70 and Q72, Q73, Q74 and Q75 to the input of a 1 of 10 decoder. The output of this decoder drives transistor switches to pull in the appropriate timing capacitors and or relay. For the fastest ramps no capacitors are pulled in. For the next range down capacitor C43 and C11 are energized via switching transistor Q79. This is accomplished by causing pin 2 of IC1 to go to -35 V which, in turn, saturates the switching transistor. In the next range relay K5 is activated and none of the capacitor ranges are pulled in. Activating this relay permanently connects capacitor C9 and C10 to the ramp timing bus. On all the remaining ranges one of the transistor switches, Q76 - Q78, is activated which, in turn, also activates the relay and maintains this part of the path in conduction. Whenever a capacitor is not in use, its potential is pulled to the -35 V level via the 1 megohm discharging resistor, R162. Since the output of this board is floating with respect to ground, some means must be provided for coupling between the floating supply and the ground reference supply. The input of the timing capacitor range circuit is a basic example of how this is accomplished. If range 1 is activated, transistor Q70 is turned on which pulls a small current from the -35 volt supply and at the same time transistor Q71 is turned on. This supplies a small amount of current to the sensing resistor, R155, which in turn causes a current to be pulled from the V_O supply via transistor Q45 to exactly balance the current necessary to couple the digital information to the range select circuitry.

(1) Amplitude Control

Transistor Q1 provides constant current bias for the amplitude vernier control whose input emitter-follower is transistor Q2. This emitter follower drives an inverter stage Q3, which provides a gain of 0.5 to the incoming signal voltage and produces the amplitude setting information referenced to the +15 V supply at the collector of Q3. Transistor Q15 is utilized to communicate the amplitude information to the floating output circuitry. This form of analog coupling provides good isolation between the two supplies since the voltage on the base of Q16

never approaches the potential of the base of Q15. Transistors Q16 and Q17 drive emitter follower Q20 to establish the amplitude level of the output circuit. The potential of the emitter Q20 is coupled to a unity gain power driver, Q21 and Q22, which supplies the clamp level for diodes CR29 and CR31, thus controlling the amplitude of the output pulse. The collector of transistor Q20 is coupled to the base network for the output current source driving transistor Q82. This circuit varies the amount of current supplied to the output stage to minimize distortion and to aid in rising the output voltage transfer function. Also connected to the collector of Q3 are two current source transistors which drive the leading and trailing edge ramp time vernier inputs.

(2) Leading Edge Vernier

The basic circuitry in this vernier operates in exactly the same manner as the input circuitry and isolation circuitry of the amplitude control. This circuitry is made up of transistors Q46, Q89, Q48, and Q52. However, unlike the amplitude control, the output of Q52 directly controls the current sink, Q53 and Q54. The programmed value of this leading-edge ramp time produces several secondary effects in the circuitry. These effects are minimized and or corrected by sampling the level of sink current that is being supplied to the timing capacitors.

Compensation for the effects of varying the leading edge program is accomplished by the two current source transistors, Q13 and Q14, whose base signal is derived from the output of the leading edge vernier isolation amplifier. Q14 applies a small correction to the amplitude circuit which minimizes the effect of changing the discharge currents and the emitter follower currents in the output amplifier chain. Transistor Q13 provides edge balance and corrects the trailing edge vernier control so there is little or no effect due to leading edge programming. The primary need for correction arises from the finite beta of the emitter follower and, hence, its change of base current with the change of emitter current.

(3) Vernier Trailing Edge Programming

The vernier trailing edge programming circuitry is essentially identical to the leading edge vernier except it is not necessary to provide any compensation networks for this function. The amplifier transistor chain consists of Q4, Q88, Q5, Q6, Q9 and Q10, whose collector is the output of the isolation amplifier and which drives Q11 and Q12, the trailing edge current source.

(4) Offset Circuitry

When a logic 1 is applied to one of the offset polarity inputs IC3 decodes the condition and turns either Q24 or Q25 off. For any condition in which both of the inputs are either a logic 1 or a logic 0, both Q24 and Q25 are left on. The output of these two transistors control saturated current switches, Q36 and Q39, which disable the offset amplifier when their associated transistor is conducting. The offset vernier control is coupled via Q31 to the base of Q33 which acts as a level shifting transistor. R94, the offset range control, in the emitter of Q33 provide the full scale adjustment for the offset circuitry. The collector of Q33 drives complementary emitter followers Q34 and Q35. These supply the appropriate signal to the current source, transistors Q41 and Q42, for the positive offset current. This offset current is coupled to the output via the inductor chain L14 and L15. When negative offset is programmed the signal from the collector of Q32 drives the emitter follower Q38 which again supplies the appropriate signal to the negative current source, transistors Q40 and Q43. These transistors supply the negative offset current for the output.

f. Power Supply

The E-H Model 1501A utilizes four nearly identical power supplies to supply the analog circuitry and a fifth supply is utilized to deliver the voltage necessary for the logic circuitry. This supply utilizes a fixed reference IC (IC301 which is located on the chassis) and an over voltage and reverse polarity protection circuit which consists of CR1 and CR2, and Q1. The IC regulator is so designed that it automatically protects itself against short circuits. However, if an over-voltage condition exists the SCR, Q1, is turned on via zener diode CR1 and its gate circuit, and effectively

crow bars the power supply to ground. If for any reason the supply is shorted to the -15 V supply, diode CR2 clamps the supply to -0.7 V. In either case the digital ICs within the instrument are protected.

The remaining power supplies are similar to the +15 V supply which consists of IC1, Q304, and the associated circuitry. The output voltage of this supply is sensed by input pin 2 of IC1 at the junction of the voltage divider made up of R6 and R7. The magnitude of the voltage at pin 2 with respect to ground is approximately 13 volts. This input produces a controlled signal at pin 10 of the IC which drives the base of the series pass transistor, Q304, whose emitter supplies the current for the +15 V supply. Before this current is passed to the supply bus, however, its magnitude is monitored via resistor R8. If the current through this resistor exceeds about 1-1/2 amps, pin 3 of the IC is moved in a negative direction which cuts off the output of IC1 turning off the series pass transistor and limiting the over-all current of the supply. A secondary protection loop exists utilizing the internal current sensing capability of this IC via the feed back to pin 4. If the base current of Q304 exceeds 100 mA, IC1 current limits and shuts down the supply. This supply is set within 1% of its nominal value at the factory and should remain within 1%.

SECTION 4

MAINTENANCE

4-1 GENERAL INFORMATION

This section of the manual gives maintenance notes and alignment procedures for the E-H Model 1501A. The instrument requires a minimum amount of maintenance; however, normal aging of electronic components may eventually cause abnormal operation. Use of the following procedures should forestall many minor malfunctions, or permit their detection before a major repair is required.

4-2 PREVENTIVE MAINTENANCE

a. Cleaning and Visual Inspection

A regular program of inspection and maintenance is recommended to minimize down-time. The operating environment and amount of usage will dictate how often the instrument should be cleaned; in the absence of more stringent conditions, inspection every four to six months is recommended. Check the instrument in the following manner:

(1) Disconnect the power cord. Inspect the exterior of the instrument for broken knobs, switches or connectors.

(2) Remove the top and bottom covers using the disassembly procedure in Subsection 4-4. If the internal surfaces and components have an excessive amount of dust deposited on them, use a low-pressure stream of air and a soft brush to remove the foreign material.

CAUTION

Do not clean the printed circuit boards with solvents, since damage to the circuits may result.

(3) Check the physical integrity of components and wiring. Look for evidence of loose connections, broken terminals, leakage of insulation compounds, and heat damage. In most cases, the source of a visually detected trouble is easily located. In the case of heat damage however, care should be taken to locate the original cause of the overheating before the instrument is put back in service.

4-3 PERFORMANCE VERIFICATION PROCEDURE

The following procedure serves as a check of the Model 1501A's functional performance and its specifications. This procedure should be used when a malfunction is suspected, or as a part of routine maintenance.

NOTE

This procedure assumes front-panel controls are used. Such controls are optional.

a. Recommended Test Equipment

The following is a list of the test equipment required for verifying operation and for calibration.

(1) Universal counter-timer capable of measuring frequency to 50 MHz and period to two seconds. Fluke Model 1952A or equivalent.

(2) Digital Voltmeter capable of measuring DC voltages to +35 V with better than 0.1% accuracy and 10 mV resolution. Fluke Model 8000A or equivalent.

(3) Sampling Oscilloscope, 350 ps risetime, digital readout, time accuracy +1%, voltage accuracy +2%, sweep speed 0.2ns/div to 100 us/div, sensitivity 100 mV/div minimum. AMC Model 1100 or equivalent.

(4) Coaxial Attenuator, 50 ohms input/out, x2 attenuation. Tektronix 017-0080-00.

(5) Coaxial Attenuator, 50 ohms input/out, x10 attenuation. Tektronix 017-0078-00.

(6) Coaxial Termination, 50 ohms. E-H part number 693-41520 (mates with AMC 1100 remote sampling probe) or equivalent.

(7) Coaxial Termination, 50 ohms, Tektronix 011-0049-01.

(8) Coaxial Cable, RG-213/U or equivalent.

(9) Male BNC to GR874 adapter, Tektronix 017-0064-00 or equivalent.

(10) Pulse Generator, E-H Model G710 or equivalent.

(11) Adapter, BNC female to dual banana plug, Tektronix 103-0040-00.

b. Frequency Range Verification

This procedure checks the operating range of the internal clock.

(1) Set all front-panel PROGRAM MODE switches to the LOCAL position.

(2) Set front-panel switches as follows:

CLOCK	INT
GATE	OFF
PULSE MODE	SINGLE
WIDTH	10 ns
DELAY	10 ns
RAMPS	999 x3 V/ns
AMPLITUDE	
POLARITY	N+
RANGE	5.0V
%of RANGE	50.00
OFFSET	OFF

(3) Connect Model 1501A trigger output to input of Universal Counter-Timer. Set Counter-Timer for frequency measurement.

(4) Measure the Model 1501A output frequency at several points on each range. The frequency should be within +5% of the setting. At low frequencies, the period mode of the Counter-Timer should be used for best resolution.

c. Width and Delay Verification.

This procedure checks the operation and calibration accuracy of the pulse width and pulse delay circuits.

(1) If a sampling oscilloscope with internal triggering is available, connect the trigger output of the Model 1501A to one channel of the oscilloscope and the main pulse output to the other channel. Connect the two coaxial attenuators in series with the sampling oscilloscope input to prevent damage to the oscilloscope. If the AMC Model 1100 is used, connect the pulse output to the oscilloscope input and the trigger output to the oscilloscope trigger input.

(2) Procedure using internally triggered oscilloscope. Trigger oscilloscope on pulse generator trigger output trace. Measure the delay between the leading edge of the trigger waveform and the leading

edge of the main pulse. The delay measured should be within $\pm 5\%$ of the setting, except on the 10 ms - 100 ms and 100 ms - 1 s ranges, where the accuracy is $\pm 15\%$. It may be necessary to use the time interval mode of the counter-timer to measure long delays. When using a sampling oscilloscope, the measurement error due to the oscilloscope must be taken into account when measuring time.

(3) Procedure using AMC 1100. Set PULSE MODE to DOUBLE. Adjust delay control Model 1100 to display trailing edge of first pulse and the entire second pulse. The pulse width may have to be adjusted to display the trailing edge of the first pulse. Set the Model 1100 to measure the time interval between the 50% points of the trailing edge of the two pulses. Measure the time interval at points on each range by setting the DELAY control. The interval measured should be within $\pm 5\%$ of the setting, except on the 10 ms - 100 ms and 100 ms - 1 s ranges, where the accuracy is $\pm 15\%$. It will be necessary to use the counter-timer as indicated above on the longer delay ranges.

NOTE

It will be necessary to change the pulse frequency as the delay setting is increased. use a frequency that will give approximately 50% duty cycle.

(4) Trigger sampling oscilloscope externally from Model 1501A trigger output. Set delay control and oscilloscope sweep time to display the entire pulse. Measure the pulse width between the 50% points on the leading and trailing edges. It should be within $\pm 5\%$ of the setting, except on the 10 ms-100 ms and 100 ms-1 s ranges, where the accuracy is $\pm 15\%$. It will be necessary to use the counter-timer to measure the width. Keep delay and width within approximately 50% of the period, as noted above.

d. Amplitude and Offset Verification

This procedure checks the operation of the amplitude and offset circuits.

(1) Set Model 1501A controls as follows:

FREQUENCY	50 kHz
DELAY	as required
WIDTH	50 ns
RAMPS	999 x 3 V/ns

PULSE MODE SINGLE
OFFSET OFF,0000V
AMPLITUDE
RANGE 10.0V
% OF RANGE 99.95

All other controls should be left in the positions specified in step b(2) above.

(2) Connect the Model 1501A pulse output (through the two coaxial attenuators in series) to the sampling oscilloscope input. Connect the trigger output to the trigger input of the oscilloscope. Trigger the oscilloscope and adjust the DELAY control so that the pulse waveform appears on the screen.

(3) Measure the peak-to-peak pulse amplitude (excluding any overshoot or ringing). It should be 10 V $\pm$ 5% (9.05 V + 10.05 V).

(4) Check the programmed amplitude at other points on the 10.0 V range. It should be within the tolerance specified.

(5) Set the RANGE switch to the other positions. The amplitude should decreased by a factor of two on each range.

(6) Set the GATE switch to the ON position. This disables the pulse output. Connect the output of the Model 1501A to the input of the digital voltmeter, using a 50-ohm termination at the digital voltmeter input.

(7) Set the OFFSET switch to POS and measure the offset voltage at several points over the range. The voltage measured should be within $\pm$ 5% of the setting.

(8) Set the OFFSET switch to the NEG and repeat step(7) above.

e. Rise and Fall Time Verification

This procedure checks the range and programming accuracy of the rise and fall ramps.

(1) Connect the output of the Model 1501A to the input of the sampling oscilloscope. Connect the two coaxial attenuators in series with the sampling oscilloscope input. Connect the trigger output to the oscilloscope trigger input.

- (2) Set Model 1501A controls as follows:

FREQUENCY	50 kHz
WIDTH	50 ns
DELAY	20 ns
AMPLITUDE	
POLARITY	N+
RANGE	10.0 V
% OF RANGE	99.95
OFFSET	OFF
GATE	OFF

Other controls should be left as in step b(2) above.

(3) Set RAMPS switch to .999 x3 V/ns. Measure 10-90% rise and fall times. WIDTH and DELAY switches may have to be adjusted to center the waveform on the screen and give a flat top on the pulse. The rise and fall times should be less than 3 ns.

(4) Set RAMPS RISE AND FALL switches to .999 V/ns. The rise and fall times should be 10.0 ns +5% +3ns (6.95 ns to 13.05 ns). Check other points within the range; the rise and fall times should be within the tolerance specified. It will be necessary to adjust width, delay and oscilloscope sweep to make the required measurement.

(5) Check all rise and fall ranges as in step (4) above.

f. Miscellaneous Function Verification

This procedure checks the external drive, gating pulse polarity, and pulse inversion functions.

(1) Connect the pulse generator to Model 1501A external drive input connector J105. Adjust pulse generator output amplitude to approximately +1.5 V.

(2) Set Model 1501A CLOCK switch to EXT position. Observe Model 1501A output and vary pulse generator frequency. The Model 1501A frequency should follow the pulse generator frequency.

(3) Set POLARITY to N-. The pulse should now be negative-going with the same baseline.

(4) Set POLARITY to I+. The pulse should now be inverted, with the pulsetop at the baseline and vice versa.

(5) Set CLOCK to INT. Connect pulse generator output to Model 1501A synchronous gate input connector J107. Monitor the main pulse output as well as the trigger output.

(6) Set GATE to ON. Adjust pulse generator output until amplitude exceeds +1.5 V. The Model 1501A output should be gated on for the duration of the gating signal and the trigger output should also be gated.

(7) Set GATE to OFF. The Model 1501A main output and trigger output should be gated off during the gate pulse.

(8) Connect pulse generator output to asynchronous gate input connector J106. Monitor main pulse output and trigger output.

(9) In both gate on and gate off operation, the main pulse output should be gated, but the trigger output should run continuously. This completes performance verification.

4-4 RECALIBRATION PROCEDURE

a. General

The recalibration procedure should be performed only when components are replaced or when the instrument fails to meet specifications. Recalibration should not be performed on a routine basis.

b. Recommended Test Equipment

The test equipment required for recalibration is the same as that required for performance verification.

c. Procedure

WARNING

When top and bottom covers are removed, hazardous voltages are exposed when primary power is connected. Use caution when working near the Power Transformer or AC Power Input.

(1) Turn Model 1501A off and disconnect primary power. Remove top and bottom covers.

(2) Set Model 1501A on its bottom and reconnect primary power. Turn instrument on and allow a 10-15 minute warmup period.

(3) Connect the digital voltmeter between ground test point and +15 V test point. Check that the voltage is +15 V $\pm$ 150 mV.

(4) Connect the digital voltmeter high side probe to the -15 V test point. Check that the voltage is -15 V $\pm$ 150 mV. If either 15 V supply is out of tolerance, R11 in the -15 V supply and R28 in the +15 V supply must be padded with 1% metal film resistors to bring the supplies into tolerance.

(5) Connect the digital voltmeter high side probe to the +5 V test point. The voltage should be +5 V $\pm$ 0.5 V.

(6) Connect the digital voltmeter between ground test point and frequency test point. Set FREQUENCY vernier switches to 0000 (range unimportant) and adjust R27 on the frequency D/A board for a reading of less than 5 mV on the digital voltmeter.

(7) Set FREQUENCY vernier switches to 4995 and adjust R30 on the frequency D/A board for a reading of 4.995 V $\pm$ 10 mV.

(8) Repeat steps (6) and (7) until no further adjustment is necessary.

(9) Repeat the procedure for delay, width, leading, trailing, amplitude, and offset D/A converters. Use 000 and maximum front-panel switch settings for adjustment, except for amplitude, which has a minimum setting of 5000. In this case the minimum setting should result in a voltage reading of less than 1 mV.

(10) Set FREQUENCY to 25.0 MHz. Connect the trigger output to frequency counter input. Set WIDTH and DELAY to 10 ns. Other control settings should be as follows:

CLOCK INT
GATE OFF
PULSE MODE SINGLE
OFFSET OFF
AMPLITUDE N+, 2.50 V, 50.00%

(11) Adjust R68 on the clock board for a frequency reading of 25.0 MHz $\pm 2\%$ (25.6 to 24.5 MHz).

(12) Set FREQUENCY to 49.95 MHz. Adjust R53 on the clock board for a frequency reading of 49.95 MHz $\pm 2\%$ (50.95 to 48.95 MHz).

(13) Set FREQUENCY to 5.00 MHz. Adjust R26 on the clock board for a frequency reading of 5.00 MHz $\pm 2\%$ (5.1 to 4.9 MHz).

(14) Repeat steps 11-13 until low, middle, and high frequencies all fall within the required tolerance.

NOTE

It is to the user's advantage to calibrate the instrument as closely as possible. The 5-50 MHz frequency range is controlled by analog circuits; the other ranges are divided digitally from this range.

(15) Turn off primary power and mount the delay and width board on an extender. Turn on primary power.

(16) Connect the output of the Model 1501A to the input of the digital readout oscilloscope. Connect the Model 1501A trigger output to the oscilloscope trigger input.

(17) Set controls as follows:

DELAY 50ns

FREQUENCY 50kHz

All other controls should be left as specified in step (10) above.

(18) Set WIDTH to 1 μ s on the 1-10 μ s range. Adjust R60 on the width and delay board for a pulse width of 1 μ s $\pm 2\%$ (1.02 to .98 μ s).

(19) Set WIDTH to 9.99 μ s on the 1-10 μ s range. Adjust R46 for a pulse width of 10 μ s $\pm 2\%$ (10.2 to 9.8 μ s).

(20) Repeat steps 18 and 19 until no further adjustment is necessary.

(21) Set WIDTH to 10 ns. Adjust R185 for a pulse width of 10 ns $\pm 2\%$ (10.2 to 9.8 ns).

NOTE

In the above steps and following steps, it is desirable to calibrate to better than 5% accuracy to allow for temperature drift and component aging.

(22) Set WIDTH to 10.0 μ s on the 10-100 μ s range and adjust R179 for a pulse width of 10.0 μ s $\pm 2\%$ (10.2 to 9.8 μ s).

(23) Set WIDTH to 99.9 μ s on the 10-100 μ s range and adjust R52 for a pulse width of 99.9 μ s $\pm 2\%$ (102 to 98 μ s).

(24) Repeat steps 22 and 23 until no further adjustment is required.

NOTE

Adjustment of R46 and R60 affects all ranges. Adjustment of R60 and R179 affects ranges 3, 5, and 7 only. Adjustment of R185 affects range 0 only.

(25) Check ranges 1, 2, 4, and 6 for error. Trimmers R46 and R60 may be readjusted to balance error on those ranges.

(26) Check ranges 3, 5, and 7 for error. Trimmers R60 and R179 may be readjusted to balance error on those ranges.

(27) Check range 0 and readjust R185 if necessary.

(28) Set PULSE MODE to DOUBLE and WIDTH TO 10.0 ns.

(29) Repeat steps 18-27 for the delay circuit, using the DELAY control wherever WIDTH is specified, and measuring the delay from the 50% point on the trailing edge of the first pulse to the 50% point on the trailing edge of the second pulse. The adjustments for delay are listed below.

NOTE

The adjustment in Step 21 is made with double pulse off and measuring from the leading edge of the T_0 output to the leading edge of the output pulse.

Step 18	-	R17
Step 19	-	R21
Step 21	-	R138
Step 22	-	R136
Step 23	-	R26
Step 25	-	R17, R21
Step 26	-	R26, R136
Step 27	-	R138

NOTE

Adjustment of R17 and R21 affects all ranges. Adjustment of R26 and R136 affects ranges 3, 5, and 7 only. Adjustment of R138 affects range 0 only.

(30) The next steps in the procedure calibrate pulse amplitude, and adjust two circuits on the power supply board using trimmers mounted on the output board. Voltages are measured with respect to the floating ground on the output board (not chassis ground). Floating ground is on pins B-T and B-16, -20 V is on pins A-S and A-15, and -35 V is on pins A-R and A-14. Adjust R201 so that the -20 V supply output is $-20\text{ V} \pm 100\text{ mV}$. Adjust R204 so that the -35 supply is $-35\text{ V} \pm 100\text{ mV}$.

(31) Set controls as follows:

PULSE MODE		SINGLE
FREQUENCY		10 kHz
DEL		200 ns
WIDTH		500 ns
AMPLITUDE		N+, 10.0V, 50.00%

(32) Measure the voltage across R20 on the output board. Record this measurement.

(33) Set % OF RANGE to 99.95. Adjust R7 on the output board for a voltage reading across R20 which is exactly twice the reading measured in step 32.

(34) Set POLARITY to N+ and % OF RANGE to 50.00. Adjust R65 for an output pulse amplitude 5.00 V.

(35) Set % OF RANGE to 99.95. Adjust R55 for an output pulse amplitude 10.0 V.

NOTE

Adjust R216 for minimum amplitude shift when changing leading edge setting from 100 to 999.

(36) Repeat steps 34 and 35 until both voltages are within the tolerances specified.

(37) The following steps calibrate the offset circuits. First, replace R175 on the output board with a 5.1 K, 1% metal film resistor. The variable resistor will be replaced with a fixed resistor later in the procedure.

(38) Set POLARITY to N- on the 10.0 V range. Terminate the Model 1501A output with the General Radio 50-ohm termination. Connect the digital voltmeter across the termination. Set the CLOCK switch to EXT.

(39) Set OFFSET +0.050 V. Adjust the zero adjust trimmer on the offset D/A board until the output is +0.050V ±5 mV.

(40) Set OFFSET to +4.995 V. Adjust the range trimmer on the offset D/A board until the digital voltmeter reads 4.995 V ±50 mV.

(41) Set OFFSET to -4.995 V. Adjust negative offset trimmer R104 on the output board for a reading of -4.995 V ±50 mV.

(42) Set OFFSET to -0.050 V. Adjust the variable resistor installed in step 37 for an output of -0.050 V ±5 mV. Remove the variable resistor and measure its resistance value. Replace the variable resistor with a 1% metal film resistor with a value closest to the measured value.

(43) Recheck output voltages with OFFSET set to + and - 0.050 V and + and - 4.995 V. Readjust trimmers if all values are not within tolerances specified.

(44) The following steps calibrate the leading and trailing edge ramp values. All measurements are made with the digital readout oscilloscope and are measured between the 10 and 90% points on the waveform. Always maintain a pulse width that will give a pulsetop which is at least 50% of the ramp time being calibrated.

(45) Set controls as follows:

FREQUENCY 6 kHz
WIDTH 30 μ s
DELAY suitable to obtain display
AMPLITUDE N+ 10.0 V 9.995
OFFSET OFF
GATE OFF
PULSE MODE SINGLE
CLOCK INT
PROGRAM LOCAL

(46) Set RAMPS to the 10 V/ μ s - 1 V/ μ s range. Set LEADING EDGE and TRAILING EDGE to 100. Adjust R34 on the output board for a leading edge reading of 8 μ s.

(47) Set LEADING EDGE to 999. Adjust R71 for a time reading of 0.8 μ s.

(48) Repeat steps 46 and 47 until no further adjustment is necessary.

(49) Set AMPLITUDE to I+ and LEADING EDGE to 100. Set TRAILING EDGE to 100 and adjust Ramp 2 Min R25 for a ramp time reading of 8 μ s.

(50) Set TRAILING EDGE to 999 and adjust Ramp 2 Max R31 for a ramp time reading of 0.8 μ s.

(51) Repeat steps 49 and 50 until no further adjustment is necessary.

(52) With TRAILING EDGE set at 100, adjust Edge Balance R57 for minimum ramp time, change when the leading edge control is moved between 099 and 999.

(53) Recheck Trailing Edge calibration and repeat steps 49 - 52.

(54) Set RAMPS to the 0.1 - 0.999 V/ns range and set both LEADING and TRAILING EDGE switches to 100. Using an insulated screwdriver, adjust trimmer capacitor C43 on the output board for equal leading and trailing edge ramp times.

NOTE

Refer to applicable options for further procedures.

4-5 TROUBLE-SHOOTING PROCEDURE

a. General

The information presented in this section is for the expressed purpose of simplifying and speeding the isolation of any fault that may occur within the instrument. Before attempting to do any major maintenance on this instrument the following test equipment should be available.

- (1) A digital voltmeter capable of making measurements to an absolute accuracy of less than 0.1%.
- (2) A sampling scope with less than 350 p sec. risetime.
- (3) Some method of parallel programming the instrument in digital form.
- (4) A pulse stimulus to drive the external gate, external drive and asynchronous gate inputs.

b. Preliminary Step

Before attempting any other maintenance on the instrument the power supply voltages should be checked to determine that they are within their specified accuracies of; $+15 \pm 0.15$ V, -15 ± 0.15 V, $+5 \pm 0.5$ V as measured on the test points on the chassis with a power supply voltage between the nominally specified limits. The output of the D/A converters should also be checked with a count of 800 on each of the D/A converters thus providing an output voltage of 4.00 ± 5 mV. Assuming these conditions are met, the following outline should help isolate the trouble.

c. No Trigger Output Pulse

For any clock vernier or range setting, if the instrument operates normally in every other respect, the problem is in the trigger output amplifier and transistors Q41, Q42, Q47, Q48, and Q49 should be checked. If there is also no output pulse the problem is in either the clock circuit, Q4 and Q5, and their associated current sources and circuitry, or

in the clock buffer amplifier, Q9 and Q10 or Q29 and Q30. A 5K sampling probe should be used to measure the waveform on the collector of Q4. This should be a square wave of approximately 1 V amplitude at the programmed frequency. If the square wave is present the signal should be followed to the amplitude chain until the fault is detected. If it is not present it is necessary to trouble-shoot the circuitry associated with these two transistors.

d. Clock Operates Correctly Only on Range 7.

Program range 6 and measure the signal on pin 8 of IC7. This should be a signal of at least 1.5 V amplitude whose base line is less than 0.5 V from ground. If the signal is not present transistor Q14, Q15, and Q18 or their associated circuitry has malfunctioned. If the signal is present check pin 11 for a low measurement. If 1 is not low then either IC12 or IC8 has malfunctioned. If it is low, check pin 8 of IC12 for a pulse whose duty cycle is 20% and whose repetition frequency is 1/10 that of the basic clock frequency. If the signal is present transistor Q35 or Q36 has failed. If the signal is not present and pin 11 is in the high state, IC12 or IC7 has failed. If pin 11 is in the low state check Q20's base which should be at approximately +5 V. If it is not at +5 V one of the divider chain, IC1 through IC6, has failed to preset and this can be determined by checking the voltage at pins 12 and 11 of these ICs. The levels should all be greater than +2 V.

e. Clock Stops On Lower Ranges.

This indicates that the divider network is not operating properly. Check to determine that the appropriate logic 1 is presented at the output of IC8 in all cases. If this does not define the problem, program in range 0 and determine that each of the decade counters is operating normally. This should isolate the problem.

f. Some Delay Ranges Missing.

Check to determine that the output of IC2 produces a logical 1 on the range that is missing. If not, IC2 is defective. If it does, determine that the transistor associated with the timing capacitor on that range is in fact saturated for the range. If not, the problem is in the chain between the output of the MC4006 and the timing capacitor's switching transistor.

g. Some Width Ranges Missing.

If the output of IC5 is producing a logical 1 on the desired range the problem is in the range switch transistor or its associated drive chain.

h. Width or Delay Ranges 3 & 5 Too Short.

For the delay IC1 is defective or transistor Q7 or Q44 is defective. For the width circuit IC6 is defective or transistor Q16 or Q49 is defective.

i. No Output Pulse From Width or Delay Board.

The following is a quick procedure to localize the problem. Determine that the clock pulse appears on connector B of the width and delay card, pins 7 and 9. These two pulses should be reciprocals of each other. If the pulse is there the clock is operating correctly and the coaxial connections are satisfactory. Check the collector of Q30 to determine that the delay one-shot is programming correctly. Use a 5 K sampling probe. If no pulse appears here the delay one-shot has malfunctioned. Check the base of Q38 to determine that the width one-shot is operating correctly. No pulse at this point indicates that the width one-shot has malfunctioned. With an output board connected determine that there are drive pulses at pins C12 and C14 of the width delay card. These pulses will be differentiated by the output board and will have an exponential character. If no pulses are present one of the following four transistors is bad or the normal inverted control circuitry has failed. Q38, Q39, Q40, and Q41 should be checked along with their associated circuitry.

j. No Output Pulse.

First, determine the width drive pulse applied to J1 and J2 is present on both connectors. Next measure the voltage across C34 and if necessary adjust R201 to produce a $-20V \pm 0.1 V$ for this supply. Next measure the voltage across C35 and adjust, if necessary, R204 to produce a $-15 \pm 0.15 V$ to this supply. If either or both of these power supplies will not adjust properly check the associated regulator on the power supply card. Next determine whether there is a negative output pulse present on the collector of the output transistors, Q62 and Q37. If this pulse is present the trouble is probably a bad balun connection or a defective relay. If the pulse is not present, observe the emitter of transistor

Q27 which should be setting at approximately -19.5 V and should be producing a negative going pulse of at least 1.5 V amplitude. This test point is easily recognized as it is the triangular shaped piece mounted above the back of the board in the middle of the assembly. If this pulse is present the problem is either in the driver or in the output transistors, the 11780's, or possibly in their current source, transistor Q83. If a pulse is present at this point, but its level is wrong, check the clamping diodes, CR29, CR30, and CR31. If no pulse appears check the base of transistor Q55 and determine that a reasonable drive pulse is present. If there is a pulse at the base of Q55, approximately 1 V amplitude, the drive amplifier is operating properly. If not, the circuit must be trouble-shot from stage to stage. If there is a pulse present at this point and there is still no output pulse, the level on the base of transistor Q27 will indicate whether the current source or the current sink is at fault and the circuitry is checked in a similar manner.

k. Calibration

If any extensive repairs are necessary to any of the modules of this instrument, that module alone should be completely recalibrated following the calibration procedure in this manual. It is not necessary to calibrate the D/A cards when repairs have been made to the functional boards and conversely when D/A cards have malfunctioned and have been replaced or repaired there is no need to recalibrate the functional module if the D/A cards are calibrated according to the procedure included in this manual.

4-6 RECOMMENDED SPARE PARTS

Table 4-1 lists the recommended spare parts required for maintenance of the Model 1501A. The first part of the list is a list of the major assemblies that may be purchased as spares by those who do not intend to repair subassemblies or components. The second part includes active electronic components and high-failure items such as relays and fuses.

See Section 5 for a complete list of all parts of the Model 1501A.

RECOMMENDED SPARE PARTS LIST

MODEL 1501ADATE January 1978

PART NUMBER	DESCRIPTION	QUANTITY USED	RECOM- MENDED SPARES	PRICE
	PRINTED CIRCUIT BOARDS			
401-29639	Power Supply Regulator Assy	1	1	
401-19977	Type B Clock Assy	1	1	
401-22373	Delay & Width Assy	1	1	
401-20458	Type C Output Assy	1	1	

RECOMMENDED SPARE PARTS LIST

MODEL 1501ADATE January 1978

PART NUMBER	DESCRIPTION	QUANTITY USED	RECOM- MENDED SPARES	PRICE
ZENER DIODES				
374-00037	1N759A	1	1	
00044	1N749A	1	1	
00080	1N747A	2	1	
11733	E-H Selected	1	1	
11761	E-H Selected	5	2	
11797	E-H Selected	9	2	
12529	E-H Selected	8	2	
DIODES				
376-00022	1N914B	82	8	
00031	1N270	5	2	
00700	MBD101	30	3	
11764	E-H Selected	13	3	
22925	E-H Selected	4	1	
MISC. PARTS				
396-00001	Fuse Holder	1	1	
398-00002	Fuse 2 Amp S.B.	1	5	
510-00020	Power Light	1	1	
584-00018	Relay Zestron 226-12-1A	1	1	
584-00019	Relay Hi G	4	1	

Table 4-1

RECOMMENDED SPARE PARTS LIST

MODEL 1501ADATE January 1978

PART NUMBER	DESCRIPTION	QUANTITY USED	RECOM- MENDED SPARES	PRICE
TRANSISTORS				
663-00070	2N3904	111	11	
00071	2N3906	103	10	
00073	2N3055	4	1	
00106	2N4919	3	1	
00107	2N4923	2	1	
00108	2N5841	1	1	
00109	2N210	3	1	
00112	MPS2369	40	4	
00115	2N4502	1	1	
00129	2N4403	12	3	
00130	2N5086	4	1	
00134	2N5089	1	1	
11724	E-H Selected	4	1	
11725	E-H Selected	2	1	
11757	E-H Selected	45	5	
11780	E-H Selected	2	1	
11781	E-H Selected	2	1	
INTEGRATED CIRCUITS				
665-00053	MC3000P	23	3	
-00057	MC4006P	4	1	
-00074	LM309K N.S.	1	1	
-00078	MC3004P	12	3	
-00079	N5741	2	1	
-00080	74145	1	1	
-00099	MC3021	5	2	

SECTION 5

PARTS LIST

5-1 ORDERING INFORMATION

Replacement parts may be ordered through an E-H Representative or directly from the factory. To be certain of receiving the proper parts, always include the following information with the order:

- a. Model number and serial number of the instrument on which the parts will be installed.
- b. Schematic reference number and subassembly name, if applicable, for which the part is intended. If the part does not have a schematic reference, the description from the parts list should be used.
- c. E-H part number.

The warranty is given on page i of this manual, opposite the Table of Contents. For factory repair, contact the Customer Service Department of E-H International, Inc., at the address given on the title page of this manual. Include the following information:

- a. Model number and serial number of the instrument on which the work is to be performed.
- b. Details concerning the nature of the malfunction; or type of repair desired.

5-2 HOW TO USE THIS PARTS LIST

The pages of this parts list correspond to the physical subsections of the instrument (printed circuit boards, chassis and subassemblies, miscellaneous hardware). Component locations can be determined from the assembly drawings and schematic diagrams in Section 6. Each component appears only once in the parts list. At the head of each page is listed the part number for the complete assembly or subassembly whose parts are listed. Care should be taken to locate malfunctions to the lowest possible level of replacement part and thus avoid the time and cost involved in "over-repair".

5-3 MAJOR ASSEMBLIES

ASSEMBLY OR PART NO.	DESCRIPTION
251-21286	Front Panel Assembly
253-21287	Rear Panel Assembly
255-21288	Chassis Assembly
257-21289	Side Panel Assembly
261-21685	Frame Assembly, 5-1/4" x 18"
401-19756	Power Supply Regulator Assembly
401-19977	Type B Clock Board Assembly
401-22373	Delay & Width Board Assembly
401-20458	Type C Output Board Assembly
401-21212	Parallel D/A Converter Assembly
820-21290	Standard Accessories
350-21710	Completion Kit, Bench 5-1/4" x 18" or
350-21764	Completion Kit, Rack Mount 5-1/4" x 18" with Slides or
350-21711	Completion Kit, Rack Mount

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ASSEMBLY NO. 1501A

E.C.O. 78-041

DESCRIPTION PROGRAMMABLE PULSE GENERATOR

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A**	253-21287	Rear Panel Assembly		1					
B									
C	255-21288	Chassis Assembly		1					
D									
E**	257-21289	Side Panel Assembly		1					
F									
G	*261-21685	Frame Assembly, 5½"x18"		1					
H									
I**	401-29639	Power Supply Reg. Bd Assy	J310	1					
J									
K	*401-19977	Type B Clock Board Assy	J301	1					
L									
M**	401-22373	Delay & Width Bd Assy	J302	1					
N									
O	401-20458	Type C Output Board Assy	J303	1					
P									
Q	820-21290	Standard Accessories		1					
R									
S	821-29876	Optional Accessories		Opt					
T									

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CHKD _____
APPD _____

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	*350-21711	Completion Kit, Rack Mount							
B		w/o Slides		1					
C									
D	822-29891	Modification Options List		Opt					
E									
F									
G									
H									
I									
J									
K									
L									
M									
N									
O									
P									
Q									
R									
S									
T									

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ASSEMBLY NO. 253-21287

DESCRIPTION REAR PANEL ASSEMBLY

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	252-22731	Panel, Rear		1					
B	144-22732	Silkscreen	Prod Ref						
C									
D	248-22734	Panel, Sub, BNC Conn. Transition		1					
E	396-0000 9	Fuse Holder	F101	1					
F	398-00025	Fuse 2½ Amp S.B.	F101	1					
G	570-00008	Fan	B101	1					
H	570-00009	Grill		1					
I	700-00204	Receptacle, AC	J101	1					
J									
K	721-00013	Connector, BNC	J102-J107	6					
L									
M		-HARDWARE-							
N	202-00311	Screw, 4-40x5/16 lg BHMS(10)	Prod Ref						
O	203-00313	Phil Dr. Screw 6-32x5/16 BHMS (10)	Prod Ref						
P	204-00008	Screw, 8-32x5/8 Lg BHMS(4)	Prod Ref						
Q	240-00001	#4-40 Kep Nut (2)	Prod Ref						
R	240-00003	#8-32 Kep Nut (4)	Prod Ref						
S	240-00002	#6-32 Kep Nut (4)	Prod Ref						
T									

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DESCRIPTION CHASSIS ASSEMBLY

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A**	254-21063	Chassis (B/M only)		1					
B									
C	258-14786	Cover, PC Conn	(J301A)	1					
D	258-13061	Cover, Terminal Strip		1					
E									
F									
G	316-00073	Cap, E1 5500 μ f 40V	C301-304	4					
H	316-00088	Cap, E1 17000 μ f 40V	C305	1					
I	318-00308	Cap, Tant 4.7 μ f 35V	C306	1					
J									
K	376-00066	Diode, 368B	CR301,302	2					
L	396-00301	Fuse Holder	XF301	1					
M	398-00034	Fuse, 8 Amp Inst	F301	1					
N									
O	405-00005	Clamp, Cap	XC301-304	4					
P	410-00034	Clamp, Cap	XC305	1					
Q	484-00023	Terminal Strip, Jumper	(TB301)	2					
R	484-00030	Card Guide		15					
S	484-00036	Terminal Strip	TB301	1					
T	484-00037	Terminal Mtg Strip		1					

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	484-00039	Card Guide		8					
B	484-00051	Termina, Feedthru		11					
C	490-00001	Transistor Mtg Kit	XQ301-305, XIC301	6					
D									
E	596-00033	Resistor 3.3Ω ½W 5%	R308	1					
F	397-00102	Resistor 1K 1W 5%	R302,304	2					
G	597-00152	Resistor 1.5K 1W 5%	R301,303	2					
H	598-00151	Resistor 150Ω 2W 5%	R305	1					
I	610-00303	Resistor 0.51Ω 12W w.w.	R307	1					
J									
K	650-19604	Transformer, Power	T301	1					
L									
M	663-00073	Transistor, 2N3055	Q301-304	4					
N	663-00115	Transistor MJ4502	Q305	1					
O	665-00074	IC LM309K N.S.	IC301	1					
P	702-21074	Cable Harness Assy, Chassis		1					
Q	700-00126	Connector, 34 Pin Header	J304	1					
R	702-21073	Wire List, Cable Harness	Prod Ref						
S	*704-23139	Coax Cable Assy, Signal							
T		Input(Output Bd) Red		1					

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	*704-23140	Coax Cable Assy, Signal							
B		Input (Output Bd) Orn		1					
C	708-21076	Delay Line, 27ns	DL301	1					
D									
E	743-00011	Connector, PC, 22 Pin Dual	J301B,C J302A,B,C						
F			J303A,B,C J305-307						
G			J308A,B J309A,B						
H			J310-314	20					
I									
J	702-21075	Wire List, Buss	Prod Ref						
K	702-21389	Wire List, Xfmr & Component	Prod Ref						
L	702-21390	Wire List, AC Pwr & Xfmr	Prod Ref						
M	702-23010	Wire List, Coax	Prod Ref						
N									
O		-HARDWARE-							
P	202-00006	Screw 4-40x $\frac{1}{2}$ BHMS (2)	Prod Ref						
Q	202-00311	Screw 4-40x5/16 BHMS(10)	Prod Ref						
R	202-00305	Screw 4-40x $\frac{1}{2}$ BHMS (41)	Prod Ref						
S	202-00310	Screw 4-40x5/16 FLTHMS(12)	Prod Ref						
T	203-00002	Screw 6-32x3/16 BHMS (2)	Prod Ref						

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	203-00008	Screw 6-32x3/8 BHMS (1)	Prod Ref						
B	203-00015	Screw #6x $\frac{1}{2}$ Type F (12)	Prod Ref						
C	203-00304	Screw 6-32x $\frac{1}{2}$ FLTHMS (4)	Prod Ref						
D	203-00313	Screw 6-32x5/16 BHMS (13)	Prod Ref						
E	205-00001	Screw 10-32x $\frac{1}{2}$ RHMS (10)	Prod Ref						
F	205-00002	Screw 10-32x3/8 BHMS (4)	Prod Ref						
G									
H	215-00002	Washer, Int Tooth #4 (8)	Prod Ref						
I	215-00010	Washer, Flat #10 (2)	Prod Ref						
J	215-00030	Washer, TFE #8 (12)	Prod Ref						
K	215-00038	Washer, TFE #10 (2)	Prod Ref						
L									
M	240-00001	Kepnut #4-40 (54)	Prod Ref						
N	240-00002	Kepnut #6-32 (16)	Prod Ref						
O	240-00004	Kepnut #10-32 (6)	Prod Ref						
P	240-00006	Nut, Hex #4-40 (1)	Prod Ref						
Q									
R	420-00006	Grommet, $\frac{1}{2}$ X3/8 (1)	Prod Ref						
S	420-00008	Grommet, 5/8x $\frac{1}{2}$ (2)	Prod Ref						
T	420-00021	Grommet, 3/8x $\frac{1}{2}$ (1)	Prod Ref						

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DESCRIPTION CHASSIS ASSEMBLY

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	460-00016	Lug, Locking #4 (2)	Prod Ref						
B	460-00301	Lug, #10 (3)	Prod Ref						
C	460-00302	Lug, Locking #10 (10)	Prod Ref						
D	475-00302	Lug, Locking #6 (1)	Prod Ref						
E									
F	500-00002	Insulator, Mica (4)	Prod Ref						
G	500-00003	Insulator, Mica T0-3(6)	Prod Ref						
H									
I									
J									
K									
L									
M									
N									
O									
P									
Q									
R									
S									
T									

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E.C.O.

ASSEMBLY NO. 257-21289

DESCRIPTION SIDE PANEL ASSEMBLY

FILLED BY DATE RELEASED TO DATE

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	256-21067	Side Panel, Left		1					
B	256-21068	Side Panel, Right		1					
C									
D									
E		-HARDWARE-							
F	203-00315	FLTHMS Screw #6-32x5/16 100° (30)	Prod Ref						
G	240-00002	Kepnut #6-32 (18)	Prod Ref						
H									
I									
J									
K									
L									
M									
N									
O									
P									
Q									
R									
S									
T									

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E.C.O.

ASSEMBLY NO. 261-21685

DESCRIPTION 5 1/4" X 18" FRAME ASSEMBLY

24 (76)

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	260-21501	Frame, Die Cast		2					
B	475-21505	Front Corner Post		2					
C	475-21514	Rear Corner Post		2					
D	425-21523	Handle		2					
E									
F	276-21540	Overlay, Handle		2					
G	240-21606	Barnut		8					
H	274-21601	Spring, Cover Lift		2					
I									
J									
K									
L									
M									
N		HARDWARE-							
O		FHTHMS 82° Screw #2-56x3/8 Lg (2)	Prod Ref						
P	215-00023	(2) #4 Washer Flat x9/32 OD	Prod Ref						
Q	215-00001	Lock Washer Int. #2 (2)	Prod Ref						
R	205-00044	Taptite Screw #10-24x3/4 LG (16)	Prod Ref						
S									
T									

DRWN _____

CHKD APC

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ASSEMBLY NO. 401-29639

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E.C.O.

DESCRIPTION POWER SUPPLY REGULATOR ASSEMBLY

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	400-29638	PC Board		1					
B	401-29639	Assembly Drawing	Prod Ref						
C	140-29640	Schematic	Prod Ref						
D									
E	311-00007	Cap, Cerm 100pf 1KV	C2,5,8,11	4					
F	311-00034	Cap, Mono .1μf 50V	C1,4,7,10	4					
G	311-00074	Cap, Cerm .01μf 100V	C13-24	12					
H	316-00062	Cap, E1 15μf 50V	C3,6,9,12	4					
I									
J	374-12529	Diode,	CR1	1					
K	376-00034	Diode, 1N4005	CR2-18	17					
L									
M	595-00101	Resistor 100Ω ½W 5%	R1	1					
N	595-00102	Resistor 1K ½W 5%	R2	1					
O	595-00302	Resistor 3K ½W 5%	R16,22	2					
P	595-00752	Resistor 7.5K ½W 5%	R3,9	2					
Q									
R	610-00307	Resistor 1.5Ω 2W w.w.	R8,15, 21,27	4					
S									
T									

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DESCRIPTION POWER SUPPLY REGULATOR ASSEMBLY

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	586-04021	Resistor 4.02K 1/8W 1% MF	R26	1					
B	586-01542	Resistor 15.4K 1/8W 1% MF	R4,10	2					
C	586-01132	Resistor 11.3K 1/8W 1% MF	R17	1					
D	586-01502	Resistor 15K 1/8W 1% MF	R5,12,23	3					
E	586-01002	Resistor 10K 1/8W 1% MF	R19	1					
F	586-07501	Resistor 7.5K 1/8W 1% MF	R6,13,25	3					
G	586-01101	Resistor 1.1K 1/8W 1% MF	R7,14,24	3					
H	586-01821	Resistor 1.82K 1/8W 1% MF	R20	1					
I									
J	586-08450	Resistor 845Ω 1/8W 1% MF	R18	1					
K									
L	663-00131	Transistor 2N4441	Q1	1					
M									
N	665-00164	IC LM723N	IC1-4	4					
O									
P									
Q									
R									
S									
T									

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ASSEMBLY NO. 401-19977

DESCRIPTION TYPE B CLOCK BOARD ASSEMBLY

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	400-19976	PC Board		1					
B	401-19977	Assembly Drawing	Prod Ref						
C	140-19978	Schematic	Prod Ref						
D	311-00009	Cap, Cerm 500pf 1KV 10%	C31	1					
E	311-00007	Cap, Cerm 100pf 1KV 10%	C13	1					
F	311-00003	Cap, Cerm 25pf	C3	1					
G	311-00010	Cap, Cerm .001μf 1KV 10%	C9,24,16 32-34	6					
H	311-00034	Cap, Cerm .1μf 50V	C2	1					
I									
J	311-00074	Cap, Cerm .01μf 100V	C1,5,7, 10-12,15,						
K			19-21,23, 27, 28	13					
L	311-00333	Cap, Dipped Mica 62pf	C4	1					
M	312-14972	Cap, Chip 0.1	C6	1					
N	318-00005	Cap, Tant 10μf 20V	C8,14,17, 18,22,29	6					
O	335-00001	Choke 1.5μh	L4-7	4					
P	335-23309	Choke Assy, 5T	L1,2	2					
Q	335-00019	Choke, .47μh	L3	1					
R	374-11761	Diode, MP	CR20A&B, CR29A&B,	2					
S	374-11732	Diode, MP 1N751A	CR33A&B	1					
T	376-00022	Diode, 1N914B	CR1-4,6-17 25-28	20					

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	376-00031	Diode, 1N270	CR 32	1					
B	376-00700	Diode, MBD101	CR5,18,19,21-24	7					
C									
D	495-00040	Socket, IC, 14 Pin	XIC7	1					
E	551-00068	Potentiometer 100Ω	R68	1					
F	551-00069	Potentiometer 100K	R26	1					
G	551-00071	Potentiometer 500Ω	R53	1					
H	595-00331	Resistor 330Ω ½W 5%	R98	1					
I	594-00100	Resistor 10Ω 1/8W 5%	R3, 7,9,62,45						
J			58,63,66,72,81,82	11					
K	594-00104	Resistor 100K 1/8W 5%	R8	1					
L	594-00150	Resistor 15Ω 1/8W 5%	R42	1					
M	594-00300	Resistor 30Ω 1/8W 5%	R6,10,14,17	4					
N	595-00100	Resistor 10Ω ½W 5%	R91,113,129						
O			130,131	5					
P	595-00101	Resistor 100Ω ½W 5%	R27,84,94,103	4					
Q	595-00103	Resistor 10K ½W 5%	R96,132126,128	4					
R	595-00121	Resistor 120Ω ½W 5%	R44	1					
S	595-00122	Resistor 1.2K ½W 5%	R61,70,	2					
T	595-00123	Resistor 12K ½W 5%	R22	1					

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DESCRIPTION TYPE B CLOCK BOARD ASSEMBLY

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	595-00102	Resistor 1K $\frac{1}{4}$ W 5%	R13,15,30,33,50,76,78,86,90,95,97,102	12					
B									
C	595-00151	Resistor 150 Ω $\frac{1}{4}$ W 5%	R12	1					
D	595-00152	Resistor 1.5K $\frac{1}{4}$ W 5%	R38,41,64,67,75,80	6					
E	595-00153	Resistor 15K $\frac{1}{4}$ W 5%	R20	1					
F	595-00182	Resistor 1.8K $\frac{1}{4}$ W 5%	R99,106	2					
G	595-00201	Resistor 200 Ω $\frac{1}{4}$ W 5%	R35,119,123,125,127	5					
H	595-00222	Resistor 2.2K $\frac{1}{4}$ W 5%	R77	1					
I	595-00240	Resistor 24 Ω $\frac{1}{4}$ W 5%	R120-122	3					
J	595-00242	Resistor 2.4K $\frac{1}{4}$ W 5%	R87-89	3					
K	595-00271	Resistor 270 Ω $\frac{1}{4}$ W 5%	R46,57	2					
L	595-00272	Resistor 2.7K $\frac{1}{4}$ W 5%	R56	1					
M	595-00302	Resistor 3K $\frac{1}{4}$ W 5%	R115, R31,32,34,73,74,114	7					
N	595-00332	Resistor 3.3K $\frac{1}{4}$ W 5%	R28,105	2					
O	595-00391	Resistor 390 Ω $\frac{1}{4}$ W 5%	R43,	1					
P	595-00392	Resistor 3.9K $\frac{1}{4}$ W 5%	R85,101	2					
Q	595-00471	Resistor 470 Ω $\frac{1}{4}$ W 5%	R29,36,37,39,116	5					
R	595-00472	Resistor 4.7K $\frac{1}{4}$ W 5%	R100,107	2					
S	596-00432	Resistor 4.3K $\frac{1}{2}$ W 5%	R16	1					
T	595-00750	Resistor 75 Ω $\frac{1}{4}$ W 5%	R117	1					

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	QTY ASSEM.	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	595-00820	Resistor 82Ω ½W 5%	R79,83	2					
B	595-00821	Resistor 820Ω ½W 5%	R111, 135	2					
C	595-00910	Resistor 91Ω ½W 5%	R65,71,92,93,109,110	6					
D	595-00912	Resistor 9.1K ½W 5%	R104	1					
E	597-00391	Resistor 390Ω 1W 5%	R59	1					
F	597-00511	Resistor 510Ω 1W 5%	R54	1					
G	595-00470	Resistor 47Ω ½W 5%	R124	1					
H	586-04020	Resistor 402Ω 1/8W 1% MF	R2,4,49,51	4					
I	586-01821	Resistor 1.82K 1/8W 1% MF	R55	1					
J	586-01003	Resistor 100K 1/8W 1% MF	R25	1					
K	586-02210	Resistor 221Ω 1/8W 1% MF	R60	1					
L	586-03321	Resistor 3.32K 1/8W 1% MF	R24	1					
M	586-05111	Resistor 5.11K 1/8W 1% MF	R23	1					
N	586-02371	Resistor 2.37K 1/8W 1% MF	R47	1					
O	586-03571	Resistor 3.57K 1/8W 1% MF	R48,52,69	3					
P	586-02001	Resistor 2K 1/8W 1% MF	R18	1					
Q	586-02211	Resistor 2.21K 1/8W 1% MF	R1,5,11	3					
R	586-01822	Resistor 18.2K 1/8W 1% MF	R21	1					
S	586-02490	Resistor 249Ω 1/8W 1% MF	R118	1					
T	586-02741	Resistor 2.74K 1/8W 1% MF	R19	1					

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DESCRIPTION TYPE B CLOCK BOARD ASSEMBLY

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ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
663-00070	Transistor 2N3904	Q11,12,17, 20,26-28						
		37-40	11					
663-00071	Transistor 2N3906	Q1,13,16, 25,43,44,						
		52	7					
663-00112	Transistor MPS2369	Q7,14,15, 18,19,21-24						
		29,30,33-36 ,49,50,51	18					
663-11757	Transistor 3640	Q2-6,8-10 31,32,41,						
		42,45-48, 53,54	18					
665-00037	IC MC849P	IC13,14	2					
665-00053	IC MC3000P	IC9-11	3					
665-00057	IC MC4006P	IC 8	1					
665-00062	IC MC 3006P	IC 12	1					
665-00076	IC MC7490P or SN7490N	IC 1-6	6					
665-00077	IC SN74196N	IC 7	1					
595-00510	Resistor 51Ω ½W 5%	R98,112, 133,134	4					

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DESCRIPTION DELAY & WIDTH BOARD ASSEMBLY

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	400-22372	PC Board		1					
B	401-22373	Assembly Drawing	Prod Ref						
C	140-22374	Schematic	Prod Ref						
D									
E	311-00005	Cap, Cerm 30pf	C4,13	2					
F									
G	311-00009	Cap, Cerm 500pf	C24	1					
H	311-00016	Cap, Cerm .001μf 1KV	C1,2,9,11, 14,18,19, 21,33-36, 38,39	14					
I									
J	311-00020	Cap, Mono .47μf/25V	C10,15	2					
K	311-00027	Cap, Cerm 820pf	C5,16	2					
L	311-00028	Cap, Cerm 200pf	C40,43	2					
M	311-00029	Cap, Cerm 330pf	C6,17	2					
N	311-00034	Cap, Mono .1μf/50V	C3,7,12, 23,37	5					
O	311-00084	Cap, Mica 130pf	C8,22	2					
P	318-00005	Cap, Tant 10μf 20V	C30-32	3					
Q	318-00042	Cap, 180μf 6V	C41,42	2					
R	320-00069	Cap, Mylar .018μf 200V	C25,29	2					
S	320-00070	Cap, Mylar 1.8μf 200V	C26,28	2					
T	320-00077	Cap, Mylar .0016μf 50V	C20,27	2					

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DESCRIPTION DELAY & WIDTH BOARD ASSEMBLY

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	335-00001	Choke 1.5 μ h	L1-3	3					
B	335-00026	Choke .33 μ h	L4-6	3					
C									
D	374-00080	Diode, 1N747A	CR15	1					
E	374-11797	Diode, MP	CR4A&B	1					
F	374-12529	Diode, Zener	CR27	1					
G									
H	376-00022	Diode, 1N914B	CR1, 18-20 30, 44, 50, 51						
I				8					
J	376-00031	Diode, 1N270	CR46-49	4					
K	376-00700	Diode, MBD101	CR13, 14, 23 25, 26, 28, 29, 31, 6						
L				9					
M	376-11764	Diode	CR2, 3, 7, 21 22, 24, 32	7					
N									
O	551-00051	Potentiometer 5K	R138, 185	2					
P	551-00070	Potentiometer 200 Ω	R17, 60	2					
Q	551-00071	Potentiometer 500 Ω	R21, 26, 46, 52	4					
R	551-00318	Potentiometer 100K	R136, 179	2					
S									
T									

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	586-01001	Resistor 1K 1/8W 1% MF	R2,134,135 186,201	5					
B	586-01002	Resistor 10K 1/8W 1% MF	R24,34	2					
C	586-01502	Resistor 15K 1/8W 1% MF	R16,59, 137,178	4					
D	586-02001	Resistor 2K 1/8W 1% MF	R3	1					
E	586-03321	Resistor 3.32K 1/8W 1% MF	R27,54	2					
F	586-03480	Resistor 348Ω 1/8W 1% MF	R18,61	2					
G	586-03571	Resistor 3.57K 1/8W 1% MF	R22,47	2					
H	586-03920	Resistor 392Ω 1/8W 1% MF	R28,55	2					
I	586-05110	Resistor 511Ω 1/8W 1% MF	R14,43	2					
J	586-08450	Resistor 845Ω 1/8W 1% MF	R20,45	2					
K									
L	595-00036	Resistor 3.6Ω 1/4W 5%	R80,97	2					
M	595-00051	Resistor 5.1Ω 1/4W 5%	R83,84,95, 96,218,219	6					
N	595-00100	Resistor 10Ω 1/4W 5%	R1,25,51	3					
O	595-00101	Resistor 100Ω 1/4W 5%	R4,6,13,33 35,42,53, 69,70,72, 93,104, 108,217	14					
P									
Q									
R									
S									
T									

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	595-00102	Resistor 1K $\frac{1}{4}$ W 5%	R31,56,111 113,116-						
B			119,121, 122,124,						
C			133,156, 167,168,						
D			175,183, 192-195,						
E			200,202, 208-210,						
F			213,216	28					
G	595-00103	Resistor 10K $\frac{1}{4}$ W 5%	R115,120, 131,140,						
H			142,144, 164,165,						
I			170,172, 173,190,						
J			191,196, 197,204-						
K			206,212, 225-229	24					
L	595-00104	Resistor 100K $\frac{1}{4}$ W 5%	R82,169	2					
M	595-00105	Resistor 1M $\frac{1}{4}$ W 5%	R125,129, 171,180,						
N			221-224	8					
O	595-00120	Resistor 12 Ω $\frac{1}{4}$ W 5%	R128,177	2					
P	595-00181	Resistor 180 Ω $\frac{1}{4}$ W 5%	R71,147,149	3					
Q	595-00153	Resistor 15K $\frac{1}{4}$ W 5%	R10,38,49, 114,132,						
R			161,188, 189,203,						
S			211	10					
T	595-00162	Resistor 1.6K $\frac{1}{4}$ W 5%	R7,37, 214,220	4					

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A	595-00182	Resistor 1.8K $\frac{1}{2}$ W 5%	R5	1					
B	595-00183	Resistor 18K $\frac{1}{2}$ W 5%	R65	1					
C	595-00200	Resistor 20 Ω $\frac{1}{2}$ W 5%	R30,98	2					
D	595-00201	Resistor 200 Ω $\frac{1}{2}$ W 5%	R73,74, 91,151	4					
E	595-00222	Resistor 2.2K $\frac{1}{2}$ W 5%	R23,48,145 146,163, 198,199						
F				7					
G	595-00241	Resistor 240 Ω $\frac{1}{2}$ W 5%	R11,41	2					
H	595-00272	Resistor 2.7K $\frac{1}{2}$ W 5%	R62,64	2					
I	595-00301	Resistor 300 Ω $\frac{1}{2}$ W 5%	R66	1					
J	595-00302	Resistor 3K $\frac{1}{2}$ W 5%	R85,100	2					
K	595-00391	Resistor 390 Ω $\frac{1}{2}$ W 5%	R101,103, 109	3					
L	595-00392	Resistor 3.9K $\frac{1}{2}$ W 5%	R207,215	2					
M	595-00431	Resistor 430 Ω $\frac{1}{2}$ W 5%	R67	1					
N	595-00471	Resistor 470 Ω $\frac{1}{2}$ W 5%	R106,230	2					
O	595-00510	Resistor 51 Ω $\frac{1}{2}$ W 5%	R15,29, 44,50	4					
P	595-00681	Resistor 680 Ω $\frac{1}{2}$ W 5%	R92	1					
Q	595-00682	Resistor 6.8K $\frac{1}{2}$ W 5%	R32,57	2					
R	595-00750	Resistor 75 Ω $\frac{1}{2}$ W 5%	R75,86,87, 148,150	5					
S	595-00752	Resistor 7.5K $\frac{1}{2}$ W 5%	R8,36,110	3					
T	595-00910	Resistor 91 Ω $\frac{1}{2}$ W 5%	R19,58	2					

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	595-00911	Resistor 910Ω ½W 5%	R9,39	2					
B	595-00912	Resistor 9.1K ½W 5%	R81,99	2					
C									
D	596-00102	Resistor 1K ½W 5%	R112,123, 130,181,						
E			182,187	6					
F	596-00122	Resistor 1.2K ½W 5%	R12,40	2					
G	596-00391	Resistor 390Ω ½W 5%	R63	1					
H	596-00361	Resistor 360Ω ½W 5%	R89	1					
I	596-00510	Resistor 51Ω ½W 5%	R107	1					
J	596-00561	Resistor 560Ω ½W 5%	R105	1					
K	596-00751	Resistor 750Ω ½W 5%	R79,88, 94,102	4					
L									
M	663-00070	Transistor 2N3904	Q1,5,9,10, 14,17,18,						
N			28,44,48, 49,53,54,						
O			55,60,64, 65,67,71,						
P			74	20					
Q	663-00071	Transistor 2N3906	Q2-4,6-8, 11,13,15,						
R			16,45,50- 52,57,62,						
S			63,68,70, 73	20					
T									

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	663-00112	Transistor MPS2369	Q12,19,25, 27,29,30,						
B			33,34,38, 39,58,59,						
C			61	13					
D	663-00129	Transistor 2N4403	Q42,43,46, 47,56,66,						
E			69,72	8					
F	663-11757	Transistor 2N3640	Q20-24,26, 31,32,						
G			35-37, 40,41	13					
H									
I	665-00057	IC MC4006P	IC2,5	2					
J	665-00078	IC MC3004P	IC1,3,4,6	4					
K									
L									
M									
N									
O									
P									
Q									
R									
S									
T									

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ASSEMBLY NO. 401-20458

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	400-20457	PC Board		1					
B	401-20458	Assembly Drawing	Prod Ref						
C	140-20459	Schematic	Prod Ref						
D									
E	311-00002	Cap, Cerm 20pf 1KV	C41,42	2					
F	311-00005	Cap, Cerm 30pf 1KV 10%	C1,10	2					
G	311-00006	Cap, Cerm 50pf 10%	C54	1					
H	311-00007	Cap, Cerm 100pf 10%	C52,53	2					
I	311-00008	Cap, Cerm 150pf 10%	C39,51	2					
J	311-00010	Cap, Cerm .001 μ f	C2,4,5, 37,45	5					
K	311-00017	Cap, Cerm .002pf	C55	1					
L	311-00034	Cap, Cerm .1 μ f 50V	C16,26,32, 33,44,46	6					
M	311-00042	Cap, Cerm .004 μ f 1KV	C3	1					
N	311-00074	Cap, Cerm .01 μ f 100V	C17,18,36, 47-50	7					
O	311-00088	Cap, Cerm 22pf	C19	1					
P	311-00097	Cap, Mica 56pf 5%	C11	1					
Q	311-00098	Cap, Mica 620pf 1%	C9	1					
R	312-14971	Cap, Chip 390pf	C13	1					
S	312-14972	Cap, Chip .1 μ f	C12,15,24, 25,38	5					
T	312-14974	Cap, Chip .01 μ f	C14	1					

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	QTY ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	318-00005	Cap, Tant 10 μ f 20V	C27-31,35	6					
B	318-00038	Cap, Tant 5.6 μ f 35V	C34,40	2					
C	320-00074	Cap, Mylar .075pf 1%	C7	1					
D	320-00076	Cap, Mylar .75pf 1%	C6	1					
E	326-00026	Cap, Poly 6750pf 1%	C8	1					
F	332-00010	Cap, Variable 2.5-9pf	C43	1					
G									
H	335-00022	Choke, 1 μ h	L17-21	5					
I	*335-10956	Choke Assy	L1,3	2					
J	*335-14686	Choke 5T (1) 4C4	L2,4,10,12	4					
K	*335-17303	Choke 10T (1) 3E2A	L11	1					
L	*335-19184	Choke 20T (2) 3D3	L13,14	2					
M	*335-23467	Choke 10T(4) 4C4	L15	1					
N	335-24784	Choke Assy	L16	1					
O									
P	361-00012	Core, 4C4	L5	1					
Q									
R	374-00037	Diode, 1N759A	CR9,56,57	3					
S	374-00044	Diode, 1N749A	CR11	1					
T	374-11733	Diode, MP 1N759A	CR12A&B	1					

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	374-11761	Diode, MP	CR7A&B	1					
B	374-12529	Diode, Zener	CR22	1					
C									
D	376-00022	Diode, 1N914B	CR1-4,6,10 14-21,23-26						
E			32-41,43	29					
F	376-22925	Diode, Sel MBD101	CR29-31,42	4					
G									
H	490-00020	Heat Sink	XQ27	1					
I	490-00041	Pad, Transistor Insulator	XQ57,58	2					
J	490-00045	Heat Sink (IERC-PA1-1CB)	XR129,XQ26 42,43,83	4					
K	490-00048	Heat Sink (Wake 26010SH5)	XQ28,59,60	3					
L	490-16574	Heat Sink Plate	XQ26	1					
M	490-17026	Heat Sink	XQ37,62	1					
N	490-17108	Heat Sink Plate	XQ37,62	1					
O	490-23128	Heat Sink Plate	XR129,XQ42, 43,83	3					
P									
Q	496-00022	Pad, Transistor	XQ27	1					
R	496-00029	Pad, Transistor		8					
S									
T	551-00038	Potentiometer 2K	R201,204	2					

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	551-00068	Potentiometer 100Ω	R71	1					
B	551-00070	Potentiometer 200Ω	R104	1					
C	551-00071	Potentiometer 500Ω	R94	1					
D	551-00073	Potentiometer 1K	R55	1					
E	551-00074	Potentiometer 2K	R7,31	2					
F	551-00075	Potentiometer 50K	R25,34,65	3					
G	551-00076	Potentiometer 500K	R57,216	2					
H									
I	584-00018	Relay, Zestron 226-12-1A	K5	1					
J	584-00019	Relay, Hi-G	K1-4	4					
K									
L	586-01001	Resistor 1K 1/8W 1% MF	R24,38,54, 84,85,93, 202,205	8					
M									
N	586-01002	Resistor 10K 1/8W 1% MF	R2,13,20, 26,39	5					
O	586-01101	Resistor 1.1K 1/8W 1% MF	R177	1					
P	586-01300	Resistor 130Ω 1/8W 1% MF	R70	1					
Q	586-01501	Resistor 1.5K 1/8W 1% MF	R53	1					
R	586-01620	Resistor 162Ω 1/8W 1% MF	R32	1					
S	586-01622	Resistor 16.2K 1/8W 1% MF	R1	1					
T	586-01822	Resistor 18.2K 1/8W 1% MF	R82	1					

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	586-01912	Resistor 19.1K 1/8W 1% MF	R212	1					
B	586-02001	Resistor 2K 1/8W 1% MF	R22,36	2					
C	586-02002	Resistor 20K 1/8W 1% MF	R28,48, 51,68	4					
D	586-02491	Resistor 2.49K 1/8W 1% MF	R52	1					
E	586-03321	Resistor 3.32K 1/8W 1% MF	R3	1					
F	586-04021	Resistor 4.02K 1/8W 1% MF	R30,203	2					
G	586-04991	Resistor 4.99K 1/8W 1% MF	R29	1					
H	586-05111	Resistor 5.11K 1/8W 1% MF	R175	1					
I	586-05621	Resistor 5.62K 1/8W 1% MF	R90	1					
J	586-07501	Resistor 7.5K 1/8W 1% MF	R176	1					
K	586-08061	Resistor 8.06K 1/8W 1% MF	R4,6	2					
L	586-09091	Resistor 9.09K 1/8W 1% MF	R81,200	2					
M	587-08870	Resistor 887Ω 1/4W 1% MF	R105	1					
N									
O	594-00039	Resistor 3.9Ω 1/8W 5%	R164	1					
P	594-00051	Resistor 5.1Ω 1/8W 5%	R128	1					
Q	594-00056	Resistor 5.6Ω 1/8W 5%	R75	1					
R	594-00103	Resistor 10K 1/8W 5%	R218	1					
S	594-00750	Resistor 75Ω 1/8W 5%	R95,110, 111,117,						
T			118	5					

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	595-00027	Resistor 2.7Ω ½W 5%	R8	1					
B	595-00036	Resistor 3.6Ω ½W 5%	R44,47	2					
C	595-00100	Resistor 10Ω ½W 5%	R40,60,72, 120,125,						
D			198,199, 214	8					
E	595-00102	Resistor 1K ½W 5%	R41,59,79, 80,86,102,						
F			154,155 169,206	10					
G	595-00103	Resistor 10K ½W 5%	R21,37, 156-158,						
H			166-168	8					
I	595-00104	Resistor 100K ½W 5%	R33	1					
J	595-00105	Resistor 1M ½W 5%	R162,163, 211	3					
K	595-00124	Resistor 120K ½W 5%	R56	1					
L	595-00152	Resistor 1.5K ½W 5%	R183,186, 188,190	4					
M	595-00182	Resistor 1.8K ½W 5%	R222	1					
N	595-00200	Resistor 20Ω ½W 5%	R61,62	2					
O	595-00201	Resistor 200Ω ½W 5%	R9	1					
P	595-00202	Resistor 2K ½W 5%	R78,91	2					
Q	595-00203	Resistor 20K ½W 5%	R10,219	2					
R	595-00222	Resistor 2.2K ½W 5%	R14,19,88, 107,150	5					
S	595-00223	Resistor 22K ½W 5%	R223-225	3					
T	595-00271	Resistor 270Ω ½W 5%	R58,165	2					

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	595-00300	Resistor 30Ω ½W 5%	R66,127	2					
B	595-00302	Resistor 3K ½W 5%	R101	1					
C	595-00330	Resistor 33Ω ½W 5%	R42,43	2					
D	595-00332	Resistor 3.3K ½W 5%	R5,92,106	3					
E	595-00333	Resistor 33K ½W 5%	R11,12,49	3					
F	595-00361	Resistor 360Ω ½W 5%	R73,74	2					
G	595-00362	Resistor 3.6K ½W 5%	R76	1					
H	595-00390	Resistor 39Ω ½W 5%	R63	1					
I	595-00391	Resistor 390Ω ½W 5%	R174,178, 208	3					
J	595-00393	Resistor 39K ½W 5%	R196	1					
K	595-00471	Resistor 470Ω ½W 5%	R191-194, 207	5					
L	595-00472	Resistor 4.7K ½W 5%	R195,197	2					
M	595-00510	Resistor 51Ω ½W 5%	R15,17,18, 99,215	5					
N	595-00511	Resistor 510Ω ½W 5%	R100	1					
O	595-00560	Resistor 56Ω ½W 5%	R112	1					
P	595-00563	Resistor 56K ½W 5%	R23,35,50	3					
Q	595-00680	Resistor 68Ω ½W 5%	R77	1					
R	595-00682	Resistor 6.8K ½W 5%	R83,87,103	3					
S	595-00683	Resistor 68K ½W 5%	R147-149, 151-153	6					
T	595-00822	Resistor 8.2K ½W 5%	R69	1					

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	595-00910	Resistor 91Ω ¼W 5%	R64	1					
B	595-00911	Resistor 910Ω ¼W 5%	R213,217	2					
C	595-	Resistor, Factory Select	R121	1					
D									
E	596-00102	Resistor 1K ½W 5%	R108	1					
F	596-00121	Resistor 120Ω ½W 5%	R113	1					
G	596-00122	Resistor 1.2K ½W 5%	R16,180, 209	3					
H	596-00390	Resistor 39Ω ½W 5%	R182,184, 187,189	4					
I	596-00681	Resistor 680Ω ½W 5%	R170-173	4					
J									
K	597-00241	Resistor 240Ω 1W 5%	R45	1					
L	597-00431	Resistor 430Ω 1W 5%	R126	1					
M	597-00621	Resistor 620Ω 1W 5%	R181	1					
N									
O	598-00131	Resistor 130Ω 2W 5%	R210	1					
P									
Q	610-00019	Resistor 100 3W w.w.	R179	1					
R	610-00136	Resistor 180 3W w.w.	R89,109	2					
S									
T	619-00006	Resistor 25.5Ω 1W MS220	R119,124	2					

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	619-00007	Resistor 51Ω 1W 1% MS210	R122,123	2					
B	621-00008	Resistor 10Ω ½W MS150	R96-98, 114-116	6					
C	622-00050	Resistor 75Ω 2W 1% MS220	R130,134	2					
D	622-00051	Resistor 150Ω 2W 1% MS220	R135,136	2					
E	622-00052	Resistor 93.1Ω 2W 1% MS220	R131-133	3					
F	622-00053	Resistor 165Ω 2W 1% MS220	R137-142, 145,146	8					
G	622-00054	Resistor 82.5Ω 2W 1% MS220	R143,144	2					
H	623-00001	Resistor 65Ω 15W 1% MP312	R129	1					
I									
J	*651-12570	Transformer	T1	1					
K	*651-19186	Transformer, Balun	T2	1					
L									
M	663-00070	Transistor, 2N3904	Q3,6,10, 13,14,17,						
N			22,24,33, 39,40,45,						
O			48,53,61, 63-66,73-						
P			75,86	23					
Q	663-00071	Transistor 2N3906	Q1,2,4,5, 11,16,20,						
R			23,25,30- 32,34,36,						
S			44,41,46, 47,52,67-						
T			72,82,84, 88,89	29					

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	663-00106	Transistor 2N4919	Q21,26,43	3					
B	663-00107	Transistor 2N4923	Q42,83	2					
C	663-00108	Transistor 2N5841	Q27	1					
D	663-00112	Transistor MPS2369	Q50,51	2					
E	663-00129	Transistor 2N4403	Q76-79	4					
F	663-00130	Transistor 2N5086	Q9,15,38,49	4					
G	663-00134	Transistor 2N5089	Q35	1					
H	663-11724	Transistor	Q12,29,85	3					
I	663-11725	Transistor	Q54,87	2					
J	663-11757	Transistor	Q7,8,18,19,55,56	6					
K	663-11780	Transistor 2N5635	Q37,62	2					
L	663-11781	Transistor	Q57,58	2					
M	663-15005	Transistor 2N5943	Q28,59,60	3					
N									
O	665-00053	IC MC3000P	IC2,3	2					
P	665-00080	IC 74145	IC1	1					
Q									
R	*704-23138	Output Cable Assembly	J108	1					
S	715-23086	Connector Strip Line		1					
T	721-00052	Connector, Micon	J1,2	2					

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	G.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	410-00020	Component Clip (1)	Prod Ref						
B	484-00051	Washer, Teflon (1)	Prod Ref						
C	060-29757	Alignment Tool	Prod Ref						
D									
E									
F									
G									
H									
I									
J									
K									
L									
M									
N									
O									
P									
Q									
R									
S									
T									

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ASSEMBLY NO. 401-21212

DESCRIPTION PARALLEL D/A CONVERTER BOARD BCD
ASSEMBLY

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ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	400-21209	PC Board		1					
B	401-21212	Assembly Drawing	Prod Ref						
C	140-21213	Schematic	Prod Ref						
D									
E	311-00001	Cap, Cerm 10pf 10V	C6	1					
F	311-00074	Cap, Cerm .01μf/100V	C1,3,5	3					
G	318-00005	Cap, Tant, 10μf 20V	C2,4	2					
H									
I	495-00059	IC Socket, 16 Pin	J1	1					
J	496-00043	Transistor Pad	XIC1	1					
K	551-00035	Potentiometer 500Ω Beckman 79PR	R43	1					
L	551-00040	Potentiometer 1K, Beckman 79PR	R40	1					
M	595-00100	Resistor 10Ω ½W 5%	R47,48	2					
N	595-00202	Resistor 2K ½W 5%	R2	1					
O	595-00165	Resistor 1.6M ½W 5%	R5	1					
P	595-00222	Resistor 2.2K ½W 5%	R3,16-39	25					
Q	595-00335	Resistor 3.3M ½W 5%	R4	1					
R	595-00394	Resistor 390K ½W 5%	R7	1					
S	595-00511	Resistor 510Ω ½W 5%	R1	1					
T	595-00682	Resistor 6.8K ½W 5%	R46	1					

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

WHERE USED 1500 Series	INDEX ☐	ASSEMBLY ☒	SPEC. ASSEM. ☐	B/M PAGE _____
	ASSEMBLY NO. <u>401-21212</u>			COPY DATE <u>3-23-73</u>
	DESCRIPTION <u>PARALLEL D/A CONVERTER BOARD BCD</u>			E.C.O. <u>77-005</u>
	ASSEMBLY			<u>77-048</u> <u>78-013</u>

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	595-00824	Resistor 820K 1/2W 5%	R6	1					
B	611-00001	Vishay Resistor 4K .05% V53-1	R15	1					
C	611-00002	Vishay Resistor 8K .1% V53-1	R14	1					
D	611-00003	Vishay Resistor 16K .1% V53-1	R13	1					
E	611-00004	Vishay Resistor 32K .1% V53-1	R12	1					
F	586-01653	Resistor 165K 1/8W 1% MF	R9	1					
G	586-03163	Resistor 316K 1/8W 1% MF	R8	1					
H	586-03321	Resistor 3.32K 1/8W 1% MF	R45	1					
I	586-06191	Resistor 6.19K 1/8W 1% MF	R41	1					
J	586-09091	Resistor 9.09K 1/8W 1% MF	R42	1					
K	586-04022	Resistor 40.2K 1/8W 1% MF	R11	1					
L	586-08062	Resistor 80.6K 1/8W 1% MF	R10	1					
M	586-04421	Resistor 4.42K 1/8W 1% MF	R44	1					
N	663-00070	Transistor 2N3904	Q1-13	13					
O									
P	665-00383	IC 74LS86	IC 6-8	3					
Q	665-00079	IC N5741	IC 1	1					
R	665-00137	IC 74LS00	IC 2-5	4					
S									
T									

JOB NO.	ASSEMBLIES REQ'D	COST CENTER	DATE

WHERE USED
1501A

INDEX ☐

ASSEMBLY ☒

SPEC. ASSEM. ☐

B/M PAGE 19

ASSEMBLY NO. 820-21290

COPY DATE 11-4-76

DESCRIPTION STANDARD ACCESSORIES

E.C.O. 77-003 78-041

77-007

77-005

77-033

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	148-07205	Manual		1					
B	786-000 20	Power Cord		1					
C	800-00032	Envelope		1					
D									
E									
F									
G									
H	146-26307	Documentation List	Prod Ref						
I									
J	276-21753	Nameplate		1					
K	276-21754	Insert, Nameplate		1					
L	276-29921	Film, Title (1)	Prod Ref						
M									
N	410-00324	Retainer, Tinnerman (2)	Prod Ref						
O									
P									
Q									
R									
S									
T									

JOB NO.	ASSEMBLIES REQ'D	COST CENTER	DATE

WHERE USED
1501A

INDEX ☐

ASSEMBLY ☒

SPEC. ASSEM. ☐

B/M PAGE 20

ASSEMBLY NO. 821-29876

COPY DATE _____

DESCRIPTION OPTIONAL ACCESSORIES

E.C.O.

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	350-21924	Mod Kit, Rack Mt Slides							
B									
C	821-21925	Accessory Kit, Extender Bds							
D									
E	1012A	Keyboard Programmer ASCII							
F									
G	5215	Digiswitch Programmer							
H		w/Power Supply, Parallel							
I									
J									
K									
L									
M									
N									
O									
P									
Q									
R									
S									
T									

JOB NO.	ASSEMBLIES REQ'D	COST CENTER	DATE

WHERE USED
MULTI

INDEX ☐

ASSEMBLY ☒

SPEC. ASSEM. ☐

B/M PAGE _____

ASSEMBLY NO. 350-21711

COPY DATE 5-11-72

DESCRIPTION RACK COMPLETION KIT 5½" x 18"

E.C.O.

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	262-21548	Bracket, Rack Mtg Ear		2					
B	258-21555	Cover, Top & Bottom		2					
C	475-21600	Spacer, Slide Mtg		2					
D									
E									
F									
G									
H									
I		-HARDWARE-							
J	203-00010	^{100°} Screw, 6-32x3/8 FLTHMS (12)	Prod Ref						
K	204-00004	Screw 8-32x3/8 BHMS (12)	Prod Ref						
L	220-00041	Nutsert 8-32 (12)	Prod Ref						
M									
N									
O									
P									
Q									
R									
S									
T									

JOB NO.	ASSEMBLIES REQ'D	COST CENTER	DATE

WHERE USED
1501A

INDEX ☐

ASSEMBLY ☒

SPEC. ASSEM. ☐

B/M PAGE _____

ASSEMBLY NO. 822-29891

COPY DATE _____

E.C.O. 78-041

DESCRIPTION MODIFICATION OPTIONS LIST

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	MKTG option Designation	QTY ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	350-21710	Mod Kit, Bench Completion							
B		5½X18	-03						
C	350-21900	Mod Kit, Fr Pnl Controls,							
D		Serial	-02						
E	350-21901	Mod Kit, Fr Pnl Controls, Parallel	-02						
F	350-21905	Mod Kit, No Clock, Ext Dr	-06						
G	350-21915	Mod Kit, GR Output Conn							
H	350-21917	Mod Kit, Output Bd Clamp							
I		Circuit							
J	350-21919	Mod Kit, IEEE Inst Buss	01-GØN						
K	350-21920	Mod Kit, ASCII BCD GndTrue	01-AØN						
L		PostTrue	01-AØP						
M	350-21921	Mod Kit, Serial BCD, 16 Bit ADDR, 16 Bit Data							
N		Gnd True	01-SØN						
		Pos True	01-SØP						
O	350-21923	Mod Kit, Opt Isol Serial BCD 3 Bit Addr,							
P		16 Bit Data GndTrue	01-SØNI						
		PostTrue	01-SØPI						
Q	350-21953	Mod Kit, Std Front Panel							
R	350-21965	Mod Kit, Parallel Prog							
S		Gnd True	01-PØN						
T		Pos True	01-PØP						

SECTION 6

DRAWINGS

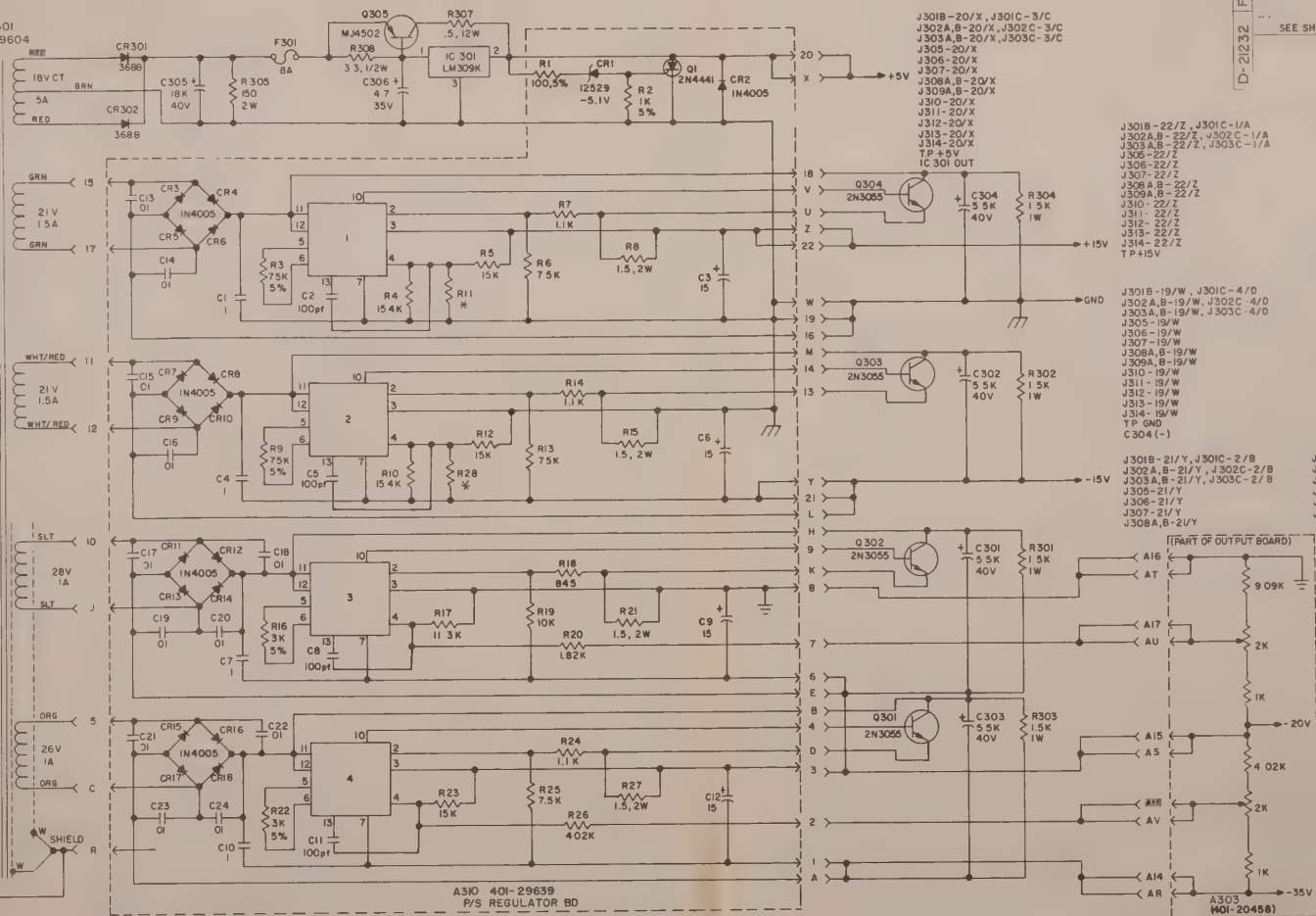
6-1 GENERAL INFORMATION

This section of the manual contains drawings of the sub-assemblies and circuits in the E-H Model 1501A Pulse Generator. The drawings contain the component circuit designators and show the location of the wiring terminals. The theory of operation is located in Section 3 and the parts list is located in Section 5.

6-2 SCHEMATIC DIAGRAMS

In the schematics, the convention of signal-flow from left to right is followed wherever practicable. Component symbology and nomenclature follow generally-accepted practices. Resistance is given in ohms. Capacitor values less than 1 are in microfarads and more than 1 are in picofarads unless otherwise labeled.

T301
650-19604



STD AC WIRING
146-21048

A310 401-29639
P/S REGULATOR BD

OUTPUT BD
J303-C & 13

J301B-20/X, J301C-3/C
J302A,B-20/X, J302C-3/C
J303A,B-20/X, J303C-3/C
J305-20/X
J306-20/X
J307-20/X
J308A,B-20/X
J309A,B-20/X
J310-20/X
J311-20/X
J312-20/X
J313-20/X
J314-20/X
TP +5V
IC 301 OUT

J301B-22/Z, J301C-1/A
J302A,B-22/Z, J302C-1/A
J303A,B-22/Z, J303C-1/A
J305-22/Z
J306-22/Z
J307-22/Z
J308A,B-22/Z
J309A,B-22/Z
J310-22/Z
J311-22/Z
J312-22/Z
J313-22/Z
J314-22/Z
TP +15V

J301B-19/W, J301C-4/D
J302A,B-19/W, J302C-4/D
J303A,B-19/W, J303C-4/D
J305-19/W
J306-19/W
J307-19/W
J308A,B-19/W
J309A,B-19/W
J310-19/W
J311-19/W
J312-19/W
J313-19/W
J314-19/W
TP GND
C304 (-)

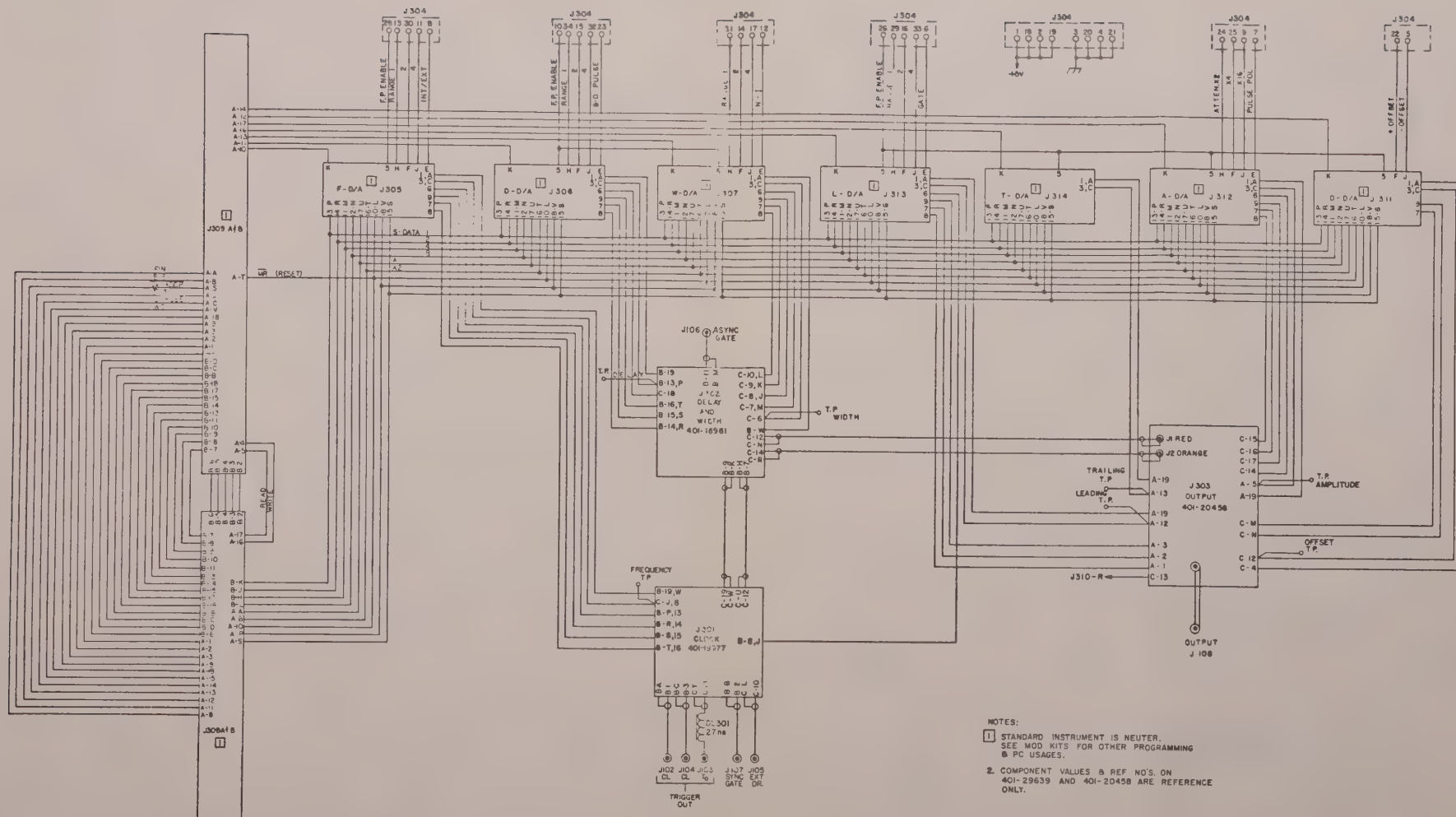
J301B-21/Y, J301C-2/B
J302A,B-21/Y, J302C-2/B
J303A,B-21/Y, J303C-2/B
J305-21/Y
J306-21/Y
J307-21/Y
J308A,B-21/Y
J309A,B-21/Y
J310-21/Y
J311-21/Y
J312-21/Y
J313-21/Y
J314-21/Y

REVISIONS

SEE SHT. 1

D-21232

PART NO.		DESCRIPTION		QTY.
MATERIAL LIST				
UNLESS OTHERWISE SPECIFIED				
E-H RESEARCH LABORATORIES, INC. DALLAS, CALIFORNIA				
TITLE				
MASTER SCHEMATIC				
REVISED BY	DATE	REVISED BY	DATE	REVISED BY
J.M.L.	10-76	J.M.L.	10-76	J.M.L.
D-21232		F		
2 of 2		2 of 2		



NOTES:

1. STANDARD INSTRUMENT IS NEUTER.
SEE MOD KITS FOR OTHER PROGRAMMING
PC USAGES.
2. COMPONENT VALUES & REF NOS. ON
40I-29639 AND 40I-20458 ARE REFERENCE
ONLY.

WASTER
SCHEMATIC

A diagram showing a vertical line with a horizontal line intersecting it. The vertical line is labeled "LUMBER" on the right side. The horizontal line is labeled "RED" on the left side. The intersection is marked with a black square. The vertical line is numbered 1 through 6 from top to bottom. The horizontal line is numbered 1 through 6 from left to right. The intersection is at the point (4, 4).

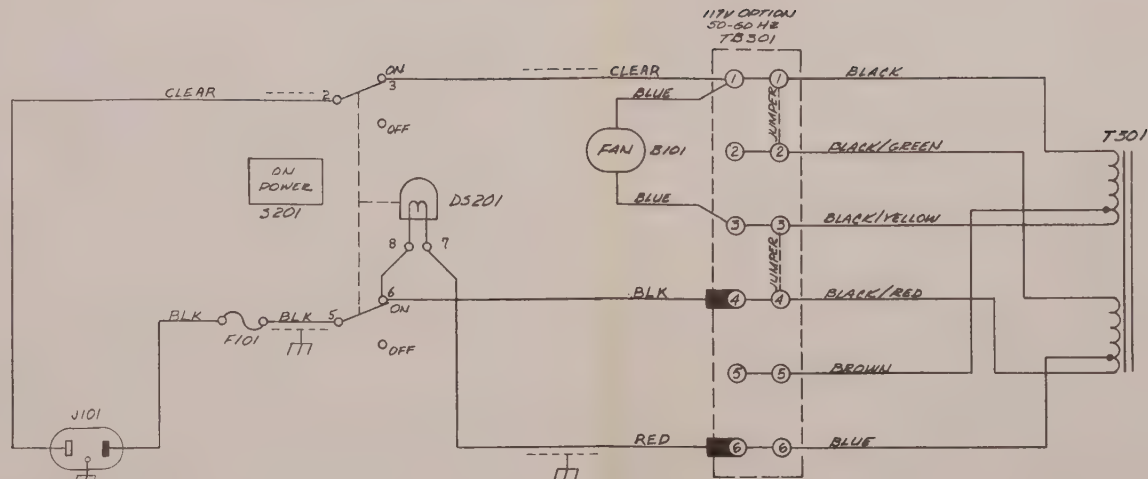
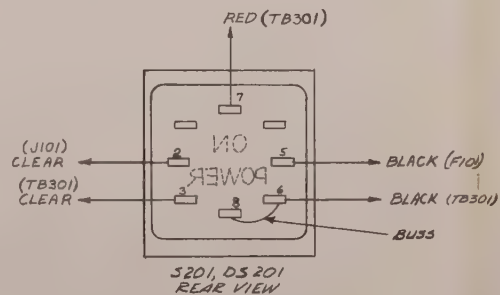


Diagram of a 6-pin connector with the following connections:

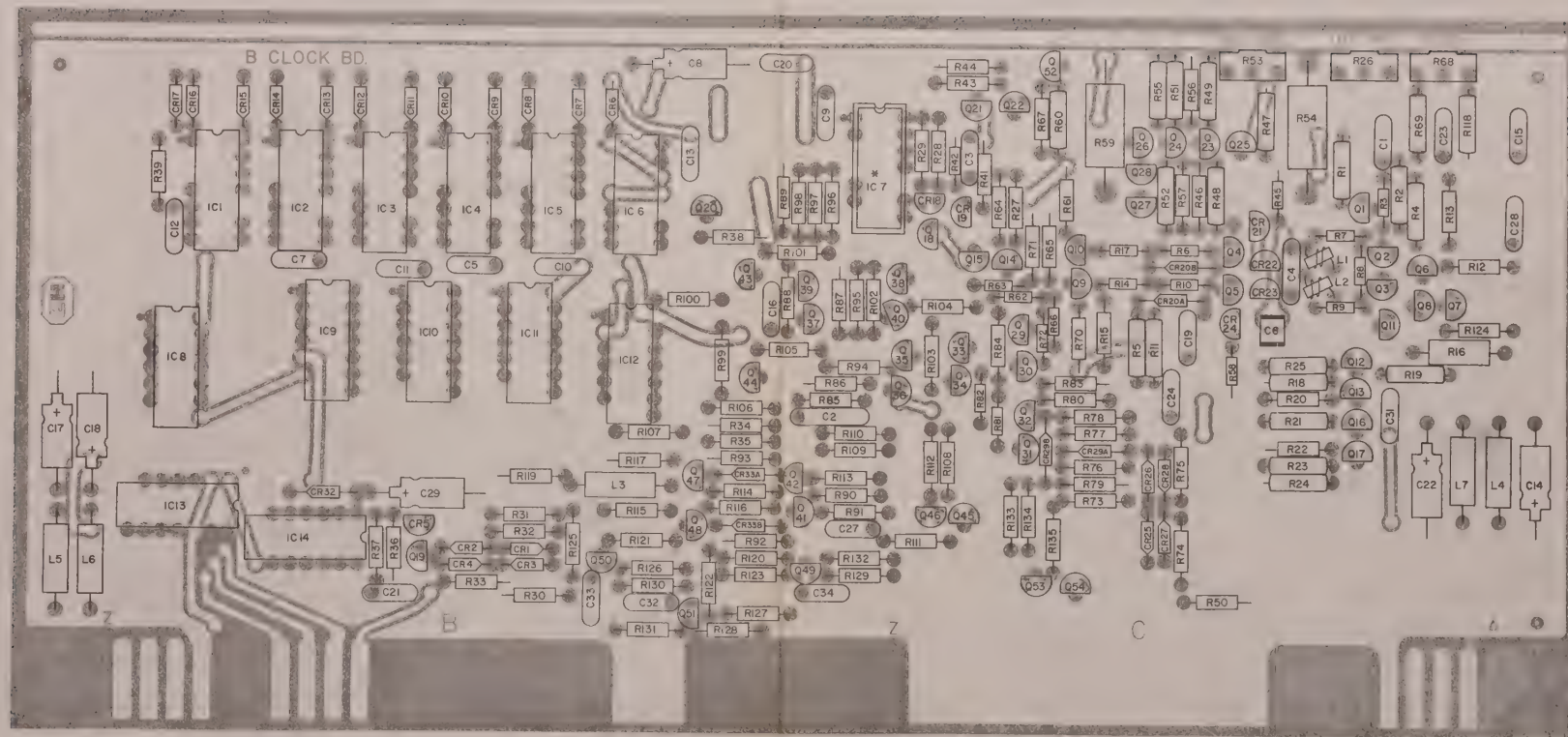
- Pin 1 connected to Pin 2
- Pin 2 connected to Pin 3
- Pin 3 connected to Pin 4
- Pin 4 connected to Pin 5
- Pin 5 connected to Pin 6

The connections are labeled: 1-2, 2-3, 3-4, 4-5, 5-6.

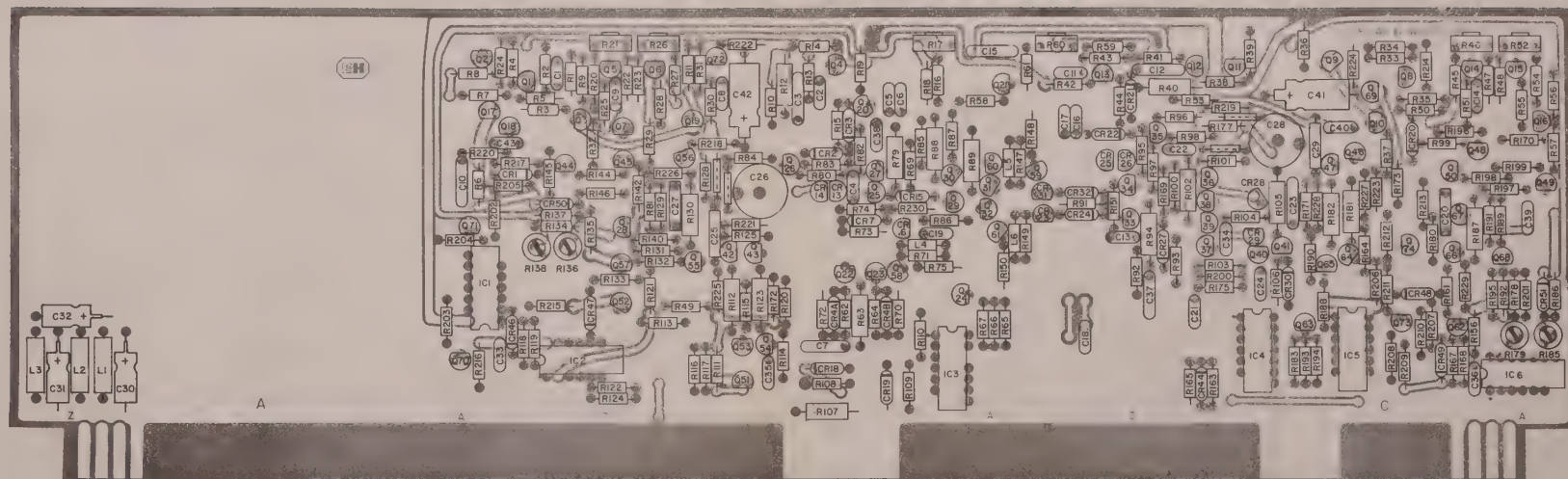
Timing diagram for the 74181 ALU showing BLK and RED signals. The diagram shows a sequence of operations: 1-1, 2-2, 3-3, 4-4 (labeled BLK), 5-5, and 6-6 (labeled RED). A vertical dashed line labeled 'JUMPER' connects the output of operation 3 to operation 5.



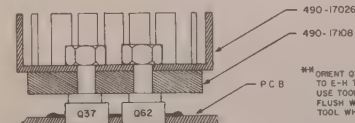
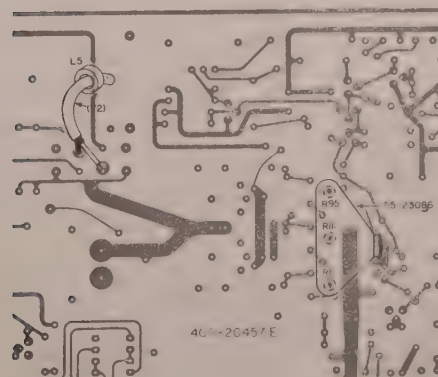
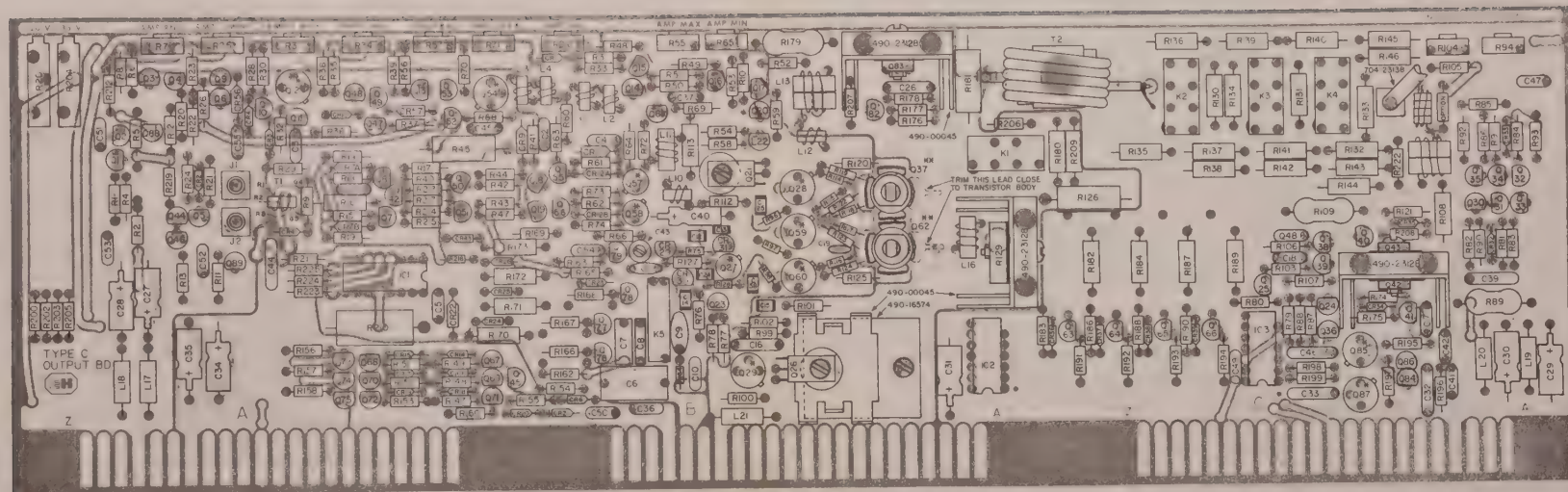
STANDARD
146-
C-21048 A



* USE IC SOCKET



ASSEMBLY DRAWING
 DELAY & WIDTH BD.
 MODEL NO: 15Q1A



** ORIENT Q37 & Q62 AND FASTEN TO E-H TOOL # 060-29757. USE TOOL TO HOLD TRANSISTORS FLUSH WITH B. PERPENDICULAR TO TOOL WHILE SOLDERING TO BOARD.

1. Q27 - USE HEAT SINK 490-00020.
2. Q28, 59, & 60 - USE HEAT SINK 490-00048.
3. Q21, 26, 42, 43, & 83 - USE TRANSISTOR MFG. KIT 500-00009.

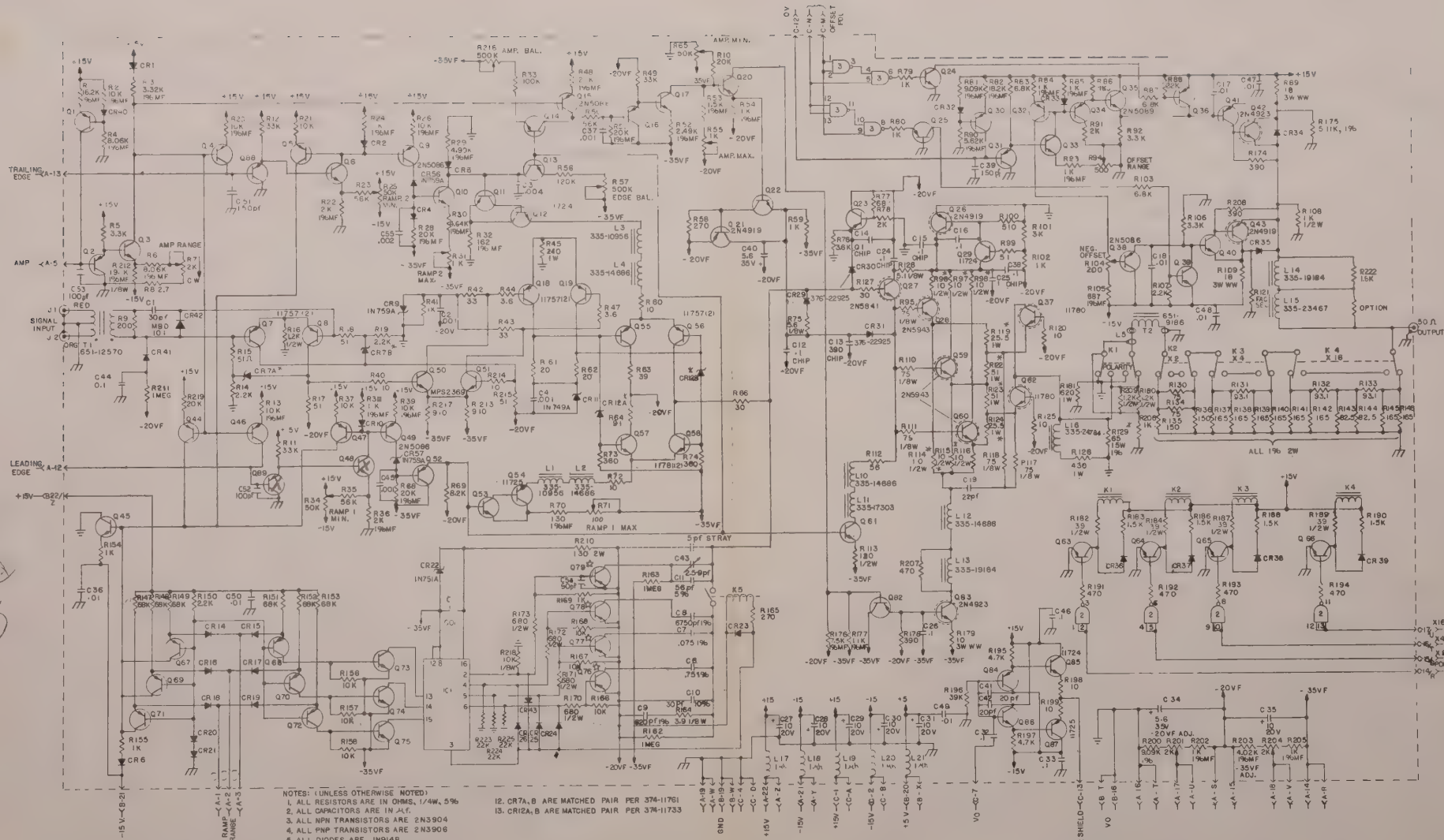
** INSTALL PAD, 490-00022, UNDER Q27. INSTALL PADS, 490-00041, UNDER Q57 & 58. INSTALL PADS, 490-00029, UNDER Q12, 28, 29, 54, 59, 60, 85, & 87. Q28, 59, & 60 MUST BE INSTALLED AFTER SOLDERING R95, 110, & 111.

ASSEMBLY DRAWING
TYPE 'C' OUTPUT BD.

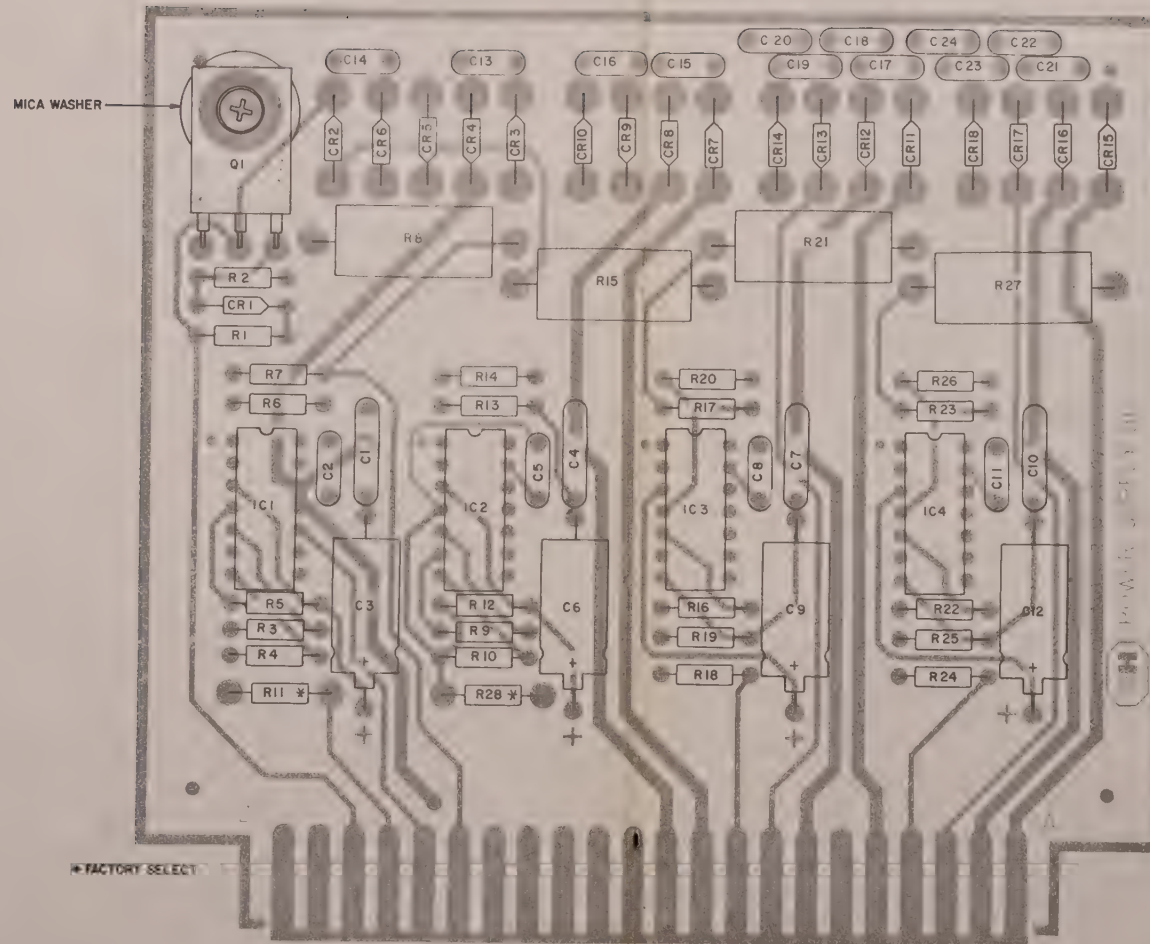
MODEL NO: 1501A

D-401-20458

E



SCHEMATIC P.C.B.
TYPE C OUTPUT BOARD



POWER SUPPLY BOARD

MODEL NO. 1501A

C- 401-29639

B

OPTION 01 GON

GENERAL PURPOSE INSTRUMENT BUS PROGRAMMING

A-1 INTRODUCTION

The General Purpose Instrument Bus (GPIB) is a worldwide standard instrument-oriented communication data bus, depending largely upon ASCII encoding of data and a 3-wire handshake for data interchange.

The Model 1500, as adapted for communication on the GPIB, can be addressed as either a "Listener" or as a "Talker." As a "Listener" it will accept program instructions for setting selected pulse parameters. As a "Talker" it reports the selected pulse parameters once, signaling END coincident with the last character. Further "handshaking" will repeat the last character and the END.

A-2 PROGRAMMING FORMAT

a. Address

A five-position Address Selector Switch can be set to any desired address. This switch, located on the rear panel of the 1500 01 GON chassis, provides both the "Listen" address and the "Talk" address. Pulse parameters are selected by addressing the 1500 as a "Listener" and sending the appropriate mnemonic; shown in Table A-1.

<u>MNEMONIC</u>	<u>FUNCTION</u>	<u>MODE CONTROL (0/1)</u>
F	Frequency	Internal/External Clock
D	Delay	Single/Double Pulse
W	Width	Inverted/Normal Pulse
L	Positive Edge	Gate OFF/Gate ON
N	Negative Edge	(Not Used)
A	Amplitude	Neg. Polarity/Pos. Polarity
O	Offset	Normal/10-20 volt (for 1504 only)
I	Initialize	

Table A-1 Pulse Parameter Mnemonics

<u>MNEMONIC</u>	<u>FUNCTION</u>	<u>MODE CONTROL</u>	<u>RANGE VALUE</u>	<u>RANGE</u>	<u>VERNIER CHARACTERS</u>
A	Atten/ Amp1		0(X128)	40-80 mv	000-999
			1(X64)	80-160 mv	
		0=Negative			
		Going Pulse	2(X32)	156-312 mv	
			3(X16)	.312-.625V	
		1-Positive			
		Going Pulse	4(X8)	.625-1.25V	
			5(X4)	1.25-2.5V	
			6(X2)	2.5-5V	
			7(X1)	5-10V	
0	Offset	Any Number (1501)	0	No Offset	
		0=Normal Amp. (1504)	2	0-+5V	000-999
		1=10-20V Amp. (1504)	4	0--5V	000-999
I	Initialize				
	Frequency 0.5 Hz, Internal Clock				
	Delay, 10 ns, Single Pulse				
	Width 10 ns, Pulse Inverted				
	Amplitude 40 mv				
	Ramp Slope Uncalibrated, Gate OFF mode				
	Offset OFF				
	All Verniers Set to 000				
	1500 Unaddressed				
	(Free-running)				

*Uncalibrated Range is a non-linear function between about 0.3 and 3.0V/ns.

**Unattenuated Ramp Slope

A-3 DETAILED OPERATION

a. Power-on State

When power is turned on, or when Initialize is sent (mnemonic I), the 1500 goes to the initial state and it is automatically not addressed.

b. Interface Clear

This signal directly and immediately Unaddresses.

c. Attention

When this signal is True (low) and DAV is True (low), commands can be received; four commands are recognized:

- (1) Prepare to Listen
X01A5A4A3A2A1 =
Addr, Listen, Atn, DAV
- (2) Prepare to Talk
X10A5A4A3A2A1 =
Addr, Talk, Atn, DAV
- (3) Unlisten
X0111111 =
?, Listen, Atn, DAV
- (4) Untalk
X10 (not addr) =
Addr, Talk, Atn, DAV

Attn, DAV does not unaddress unless either:

- (a) Another instrument's Talk address is placed on the line, or
- (b) the Unlisten command "?" is placed on the line.

d. Translation to the 1500 Bus From the GPIB

The 1500 internal bus is a 4-bit bidirectional party line bus. Functions programmed on this bus must be selected by mnemonic and properly formatted. The first 4-bit character is a combination Range and Mode character. This combination is compiled by first loading the Mode character into a latch, then enabling this latch at the same time that the Range character is placed on the lines.

Since this Mode Switch is necessarily loaded into the latch whenever we have had Select Mode for one character clock, and since we only get Select Mode immediately following the appearance of a function mnemonic, it is possible both to program the same function with a number of different values without ever Unlistening, and to use abbreviated commands that consist of "Listen, new value, Unlisten" sequence. Whenever the signal READY TO TALK is true, the output drivers are enabled. If NRFD and NDAC were both high when the 1500 was instructed to talk, the instrument waits for Listener. To read back a complete pulse parameter program when ad-

dressed as a Talker, it is necessary for the 1500 to have first been sent a Mode Selection mnemonic while addressed as a Listener. The Select Mode latch will be set and the 1500 will then be able to send five characters, a Mode Switch value followed by the 4-digit Function value. If select Mode is True, data bits 0-2 are gated off the bus, and bit 3 is gated to DIO1 to transmit the Mode Switch value.

e. Listening

Once the 1500 is addressed as Listener, the next step is selecting the function. This is done by the appropriate mnemonic. If a mnemonic is entered, the least significant three digits are stored in a latch. The latch output is decoded to select the proper register on the bus and SELECT MODE is set.

When Atn is removed; NRFD goes high. Soon, depending on the talker, DAV goes low. If the character being transmitted is an ASCII integer (0-9), then CHARCLK will be enabled. DAV low then drives CHARCLK high, clocking the data on DIO1 into the MODE SWITCH. It also sets NRFD low and releases NDAC. Then, when DAV goes high, CHARCLK goes low, toggling the MODE SWITCH, and pulling down NDAC. Shortly, thereafter, NRFD goes high. Soon, DAV goes low, driving CHARCLK high. This time, however, the signal passes through to NWRTCK, loading the multiplexed Range and Mode Switch data into the first character position of the selected register. This also releases NDAC and pulls NRFD low. The, DAV goes high, pulling down CHARCLK and incrementing the address counter which permits loading of the first vernier character.

Any number of successive characters may now be loaded. They will be entered as Range, Vernier MSD, Vernier NMSD, Vernier LSD, Range, Vernier MSD, etc. This permits cycling the 1500 through many successive Range and Vernier values for a given function without further addressing. To program another function, simply send the appropriate mnemonic, then the character sequence "Mode Switch, Range, Vernier, Vernier, Vernier".

Since the 1500 is designed to permit both multiple Range-Vernier settings and to permit sending pulse parameters for any number of functions in a single string, there is no need for an End-of-String character or END message. A new function mnemonic at any point resets the Mode Switch and Character Address Counter.

f. Talking

The 1500 must be addressed as Listener and sent the appropriate mnemonic in order to read the program back. The proper sequence is "Listen, Mnemonic, Talk," (read pulse parameters). The first character sent will be the Mode Switch for the selected mnemonic. It will be either ASCII Zero or One. The next character sent will be the Range. Three more characters, the Vernier values, complete the message. Coincidentally with the last Vernier Digit, the END message is sent, indicating to the Listener and the Controller that the message is complete. The last four characters, together with the END message on the last character, are repeated until the 1500 is addressed as a Listener and a new mnemonic is sent. Carriage Return and Line Feed are not transmitted by the 1500.

JOB NO.	ASSEMBLIES REQ'D	COST CENTER	DATE

WHERE USED

1501A
1504

INDEX ☒

ASSEMBLY ☐

SPEC. ASSEM. ☐

B/M PAGE _____

ASSEMBLY NO. 350-21919

COPY DATE 3-28-78

E.C.O. 78-041

DESCRIPTION MOD KIT, GPIB INTERFACE

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	QT. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A									
B									
C		ADD TO INDEX							
D	**401-22619	D/A Serial Board Assy	J305-307, J311-314	7					
E	**401-27508	GPIB Interface Bd Assy	J309	1					
F									
G		ADD to REAR PANEL ASSY							
H	**249-29662	Sub Panel, Rear Assy		1					
I									
J		ADD to Chassis Assy							
K	702-29666	Wire List, Mod	Prod Ref						
L									
M		ADD to Standard Accessories							
N	146-26275	Documentation List	Prod Ref						
O	706-00001	Cable, IEEE 488-1975		1					
P									
Q									
R									
S									
T									

NOTE: MARKETING OPTION 01-GØN
**SEE 1500 Series

JOB NO.	ASSEMBLIES REQ'D	COST CENTER	DATE

WHERE USED 1500 Series	INDEX ☐	ASSEMBLY ☒	SPEC. ASSEM. ☐	B/M PAGE _____
	ASSEMBLY NO. <u>249-29662</u>			COPY DATE <u>1-10-77</u>
	DESCRIPTION <u>SUB PANEL, REAR ASSEMBLY</u>			E.C.O. <u>77-013</u>
				<u>77-047</u>

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	O.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	252-27722	Rear Sub Panel		1					
B	144-27723	Silkscreen, Rear Sub Pnl	Prod Ref						
C	706-29698	GPIO Cable Assy		1					
D									
E	700-29520	Standoff, Short Stud		2					
F									
G		-HARDWARE-							
H	202-00012	Screw 4-40x3/8 BHMS (2)	ProdRef						
I	240-00002	Kepnut 6-32 (2)	Prod Ref						
J									
K									
L	215-00053	Washer Split Lock #10 (2)	Prod Ref						
M									
N									
O									
P									
Q									
R									
S									
T									

JOB NO.	ASSEMBLIES REQ'D	COST CENTER	DATE

WHERE USED
1500 Series

INDEX ☐

ASSEMBLY ☒

SPEC. ASSEM. ☐

B/M PAGE _____

ASSEMBLY NO. 401-27508

COPY DATE 3-22-78

DESCRIPTION G.P.I.B. INTERFACE BOARD ASSEMBLY

E.C.O. 78-048

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	400-27507	PC Board		1					
B	401-27508	Assembly Drawing	Prod Ref						
C	140-27509	Schematic	Prod Ref						
D									
E	311-00074	Cap, Cerm .01 μ f 100V	C3-31	29					
F	318-00005	Cap, Tant 10 μ f 20V	C2	1					
G	318-00021	Cap, Tant 5.6 μ f 20V	C1	1					
H									
I	335-00022	Choke, 1 μ h	L1	1					
J									
K	376-00022	Diode, 1N4448	CR1,2	2					
L									
M	595-00102	Resistor 1K $\frac{1}{2}$ W 5%	R2-5, 10-12 16-20, 5						
N			54-56	15					
O	595-00104	Resistor 100K $\frac{1}{2}$ W 5%	R1	1					
P	595-00152	Resistor 1.5K $\frac{1}{2}$ W 5%	R6-9	4					
Q	595-00302	Resistor 3K $\frac{1}{2}$ W 5%	R37-52	16					
R	595-00331	Resistor 330 Ω $\frac{1}{2}$ W 5%	R14, 15	2					
S	595-00471	Resistor 470 Ω $\frac{1}{2}$ W 5%	R53	1					
T	595-00622	Resistor 6.2K $\frac{1}{2}$ W 5%	R21-36	16					

JOB NO.	ASSEMBLIES REQ'D	COST CENTER	DATE

WHERE USED
1500 Series

INDEX ☐

ASSEMBLY ☒

SPEC. ASSEM. ☐

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ASSEMBLY NO. 401-27508

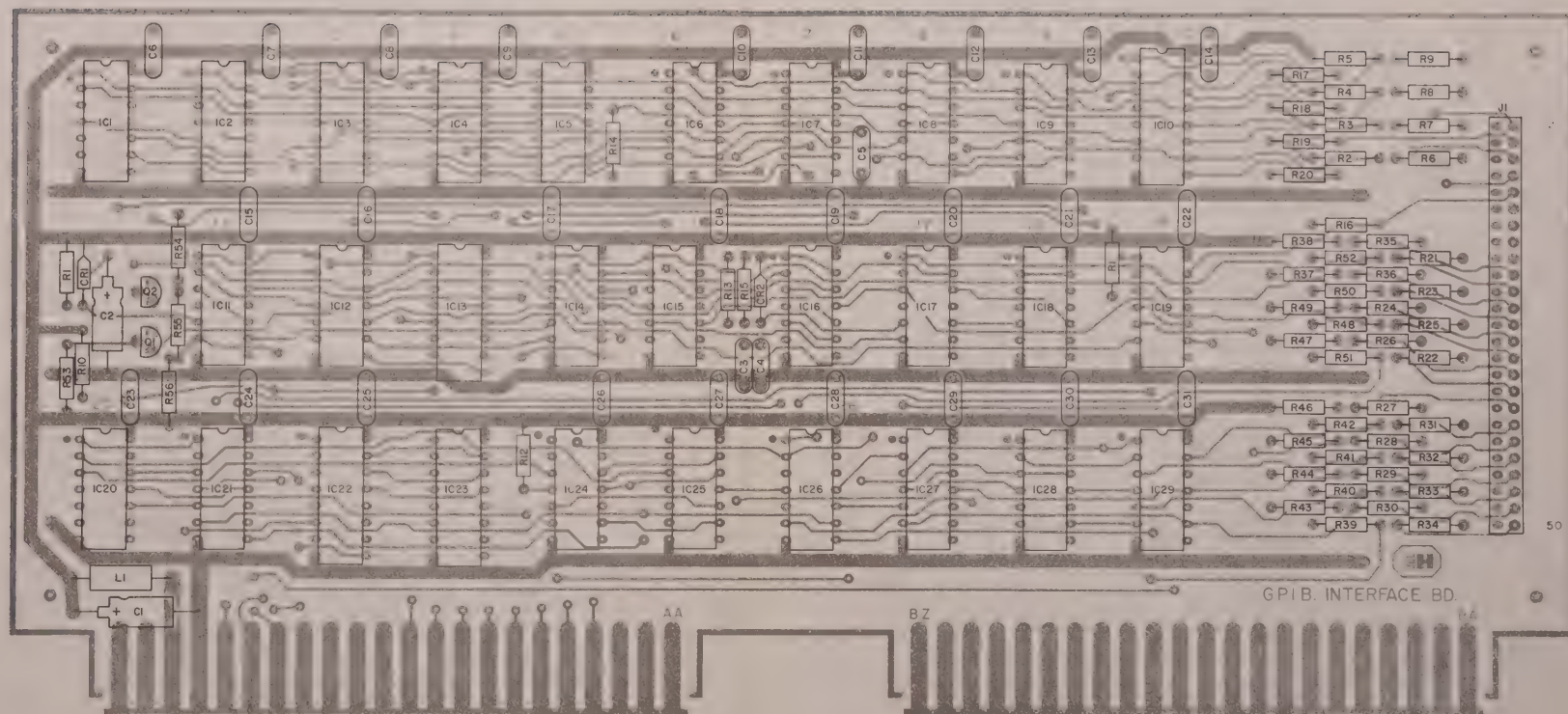
COPY DATE 10-12-78

E.C.O. 78-048

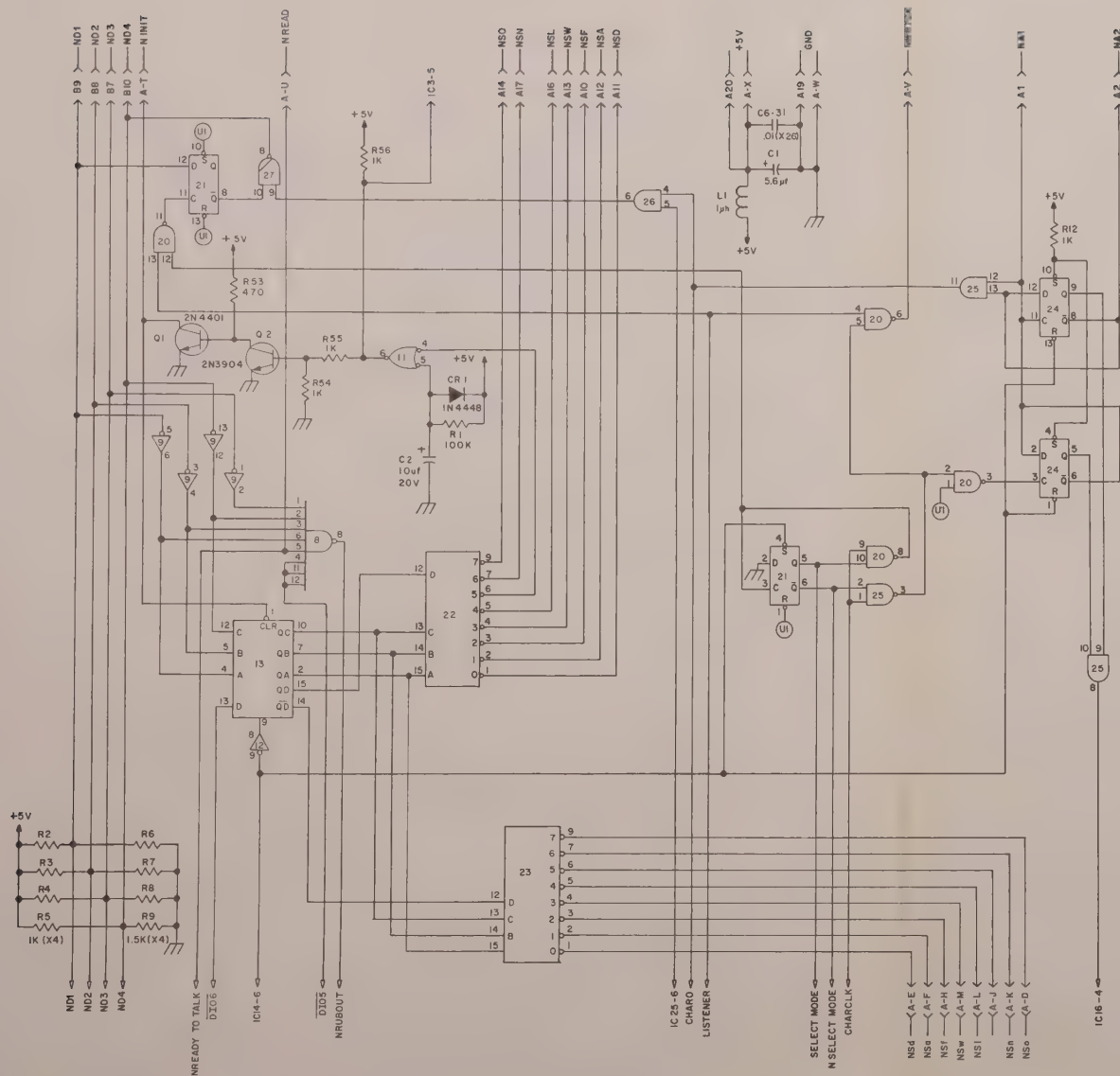
DESCRIPTION G.P.I.B. INTERFACE BOARD ASSEMBLY

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	663-00070	Transistor 2N3904	Q2	1					
B	663-00124	Transistor 2N4401	Q1	1					
C									
D	665-00024	IC SN7400N	IC5,14,20	3					
E	665-00025	IC SN7410N	IC4,7	2					
F	665-00050	IC SN7402N	IC15	1					
G	665-00085	IC MC7404P	IC6,9,12	3					
H	665-00088	IC SN7420N	IC1-3	3					
I	665-00089	IC SN7442N	IC22,23	2					
J	665-00090	IC SN7430N	IC8	1					
K	665-00094	IC MC7401P	IC28	1					
L	665-00155	IC SN7438N	IC16,18,27	3					
M	665-00183	IC SN74175N	IC13	1					
N	665-00189	IC SN7486N	IC19	1					
O	665-00190	IC SN7408	IC11,25,26	3					
P	665-00197	IC SN7474N	IC21,24	2					
Q	665-00198	IC SN7485N	IC10	1					
R	665-00237	IC SN7414N	IC17,29	2					
S									
T	700-00283	Connector, 50 Pin Berg	J1	1					



ASSEMBLY DRAWING
G.P.I.B. INTERFACE BD.
MODEL NO: 1500



REF. DESIG.	IC'S	TYPE	POWER PINS
1, 2, 3	SN7420N	14	7
5, 14, 20	SN7400N	14	7
6, 9, 12	SN7404N	14	7
4, 7	SN7410N	14	7
8	SN7430N	14	7
10	SN7485N	16	8
11, 25, 26	SN7408N	14	7
15	SN7402N	14	7
16, 18, 27	SN7436N	14	7
17, 29	SN7414N	14	7
19	SN7486N	14	7
21, 24	SN7474N	14	7
22, 23	SN7442N	16	8
13	SN74175N	16	8
28	SN7401N	14	7

NOTES—
 1. RESISTORS ARE 1/4 W, 5%, C.C.
 2. CAPACITORS ARE IN μ F.
 3. REF. DWGS.:
 FAB.: 400-27507
 ASS'Y: 401-27508
 4. J1 IS SCOTCHFLEX 3433-2002

SCHEMATIC,
 G.P.I.B. INTERFACE BD.

APPENDIX A-2

OPTION 01 SOPI
SERIAL BY WORD ISOLATED

I PROGRAMMING SPECIFICATIONS

a. Format

Serial by word program format with three-bit function address and 16-bit data word. See Table 1-1.

b. Logic Levels

Positive true; logic "0" 0 to +.05 V; logic "1" +4.5 to +5 V. Input logic uses separate address and data freed-through connectors on rear panel. Logic lines optically isolated from internal chassis ground and internal voltage references.

c. Vernier Programming

Each set of vernier connections is made up of three digits in 8-4-2-1 BCD form. Width and delay programming is straightforward; the number programmed in BCD form is the required value. For example, a pulse width of 172 μ s is a vernier value (in BCD) of 172. Frequency, amplitude, and offset require transformation from the desired value to the correct vernier. These functions will be discussed in the following paragraphs.

d. Frequency Programming

Because the frequency ranges do not have end points which are even decades, the required vernier is found by multiplying the desired frequency by a factor of two and taking the three most significant digits as the vernier. For example, a pulse repetition frequency of 452.3 kHz multiplied by two gives a value of 904.6 and a vernier program of 905.

e. Amplitude Programming

The basic (unattenuated) amplitude range is 5 V with 000 vernier and 9.99 V with 999 vernier. To determine the vernier for a given amplitude, including attenuation, use the formula below:

$$\text{Ampl. Vernier} = \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation})^{-5}}{.005}$$

f. Offset Programming

The range of offset programming is from 0 to 5 V. The vernier program is the required offset value in volts, multiplied by 200. For example, if the required offset is 200 mV, the vernier is 200×0.2 , or 040.

g. Leading & Trailing Edge Ramps

Since the leading and trailing edge ramps of the Model 1501A are constant slope with respect to changes in amplitude vernier, and constant risetime with respect to changes in attenuation, a calculation must be made to determine the program for a given combination of amplitude and rise/fall time. The fastest leading and trailing edge times are obtained at a vernier of 999, and the slowest times at a vernier of 100. To determine the proper vernier, use the following formula:

$$\text{Ramp Rate} = \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) \times K}{\text{Rise of Fall Time}}$$

Where "K" = .8 for 10-90%, K = .6 for 20-80%, etc.

II SAMPLE PROGRAM

Required Amplitude: 800 mV

Required 10-90% risetime: 20 ns

Step 1. Determine attenuation value by inspecting Table 1-2. An 800 mV output will be obtained on Range 4 which has an attenuation value of 8.

Step 2. Set attenuator to Range 4.

Step 3. Determine amplitude vernier setting using the attenuation value found in Step 1.

$$\begin{aligned} \text{Ampl. Vernier} &= \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) - 5}{.005} \\ &= \frac{(.800) \times (8) - 5}{.005} \\ &= 280 \end{aligned}$$

Step 4. Set Amplitude vernier to 280.

Step 5. Determine ramp rate using:

$$\begin{aligned}
 \text{Ramp Range} &= \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) \times K}{\text{Risetime}} \\
 &= \frac{(.800) \times (8) \times .8}{200 \text{ ns}} \\
 &= \frac{5.12 \text{ V}}{20 \text{ ns}} \\
 &= \frac{5.12 \text{ V}}{.02 \mu\text{s}} \\
 &= 256 \text{ V}/\mu\text{s} = 0.256 \text{ V/ns}
 \end{aligned}$$

By inspecting Table 1-2, we find that a ramp rate of .256 V/ns can be obtained with Ramp Range = 1.

Step 6. Set Ramp Range to 1.

Step 7. Set Ramp Vernier to 256.

NOTE

Since the vernier only varies between counts of 100 to 999, it may be necessary to multiply the Ramp Rate by either 10 or 100 to obtain the 3-digit vernier setting. Example: if Ramp Rate = 24 V/ μ s, then Vernier = 24 $\times$ 10 = 240. Example: if Ramp Rate = 1.3 V/ μ s, then Vernier = 1.3 $\times$ 100 = 130.

III RESET MODES

When primary power is turned on, all internal storage is reset to zero, and the Model 1501A is in the following modes: maximum attenuation, inverted pulse mode, negative pulse, zero offset, Gate OFF mode, frequency, delay, width, rise and fall times at minimum, internal clock, and single pulse. After initial programming, reset of internal storage can be accomplished by activating the Master Reset line on pin 1 of rear-panel connectors J110/J111. Master Reset is activated in the low state.

IV DATA & ADDRESS TIMING

Timing and calibration of data/address and strobe inputs are shown in Figure D-3.

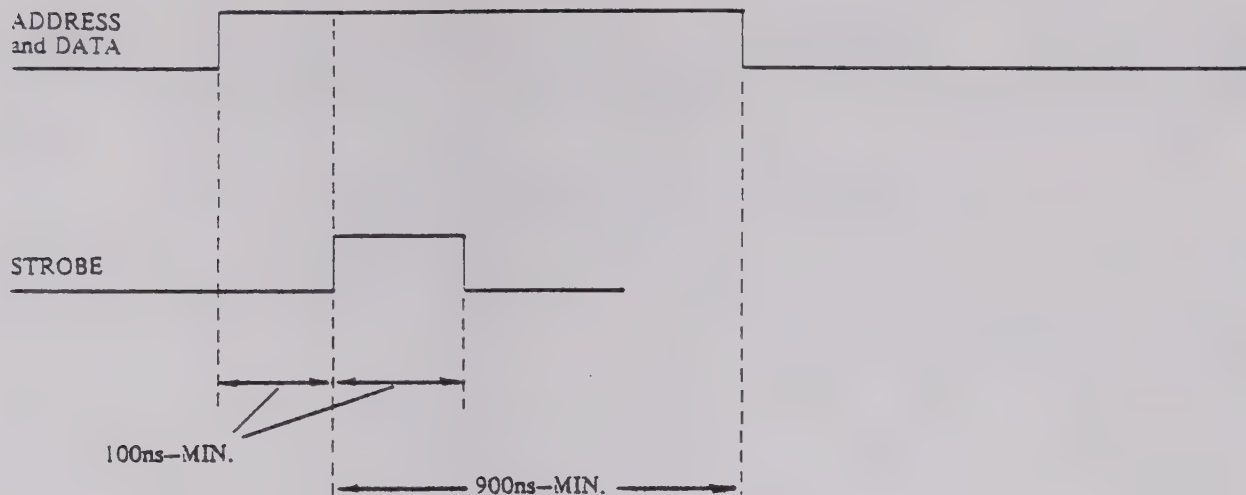
ADDRESS - J110 and J111

Pin	Signal	Pin	Signal
1	Master Reset	22	Gate Mode
2	2 ⁰ Addr. Bit	23-24	Not used
3	2 ¹ Addr. Bit	25	+5 V input-LED common
4	2 ² Addr. Bit	26-41	Logic Common (not tied to chassis ground)
5-18	not used		
19	Strobe	42-49	Open - may be used for feedthrough signals
20-21	not used	50	+5 V input-LED common

DATA - J112 and J113

Pin	Signal	Pin	Signal
1	not used	18-24	not used
2	2 ⁰	25	+5 V input-LED common
3	2 ¹	26-41	Logic Common (not to chassis ground)
4	2 ²	42-49	Open - may be used for feedthrough signals
5	2 ³	50	+5 V input - LED common
6	2 ⁴		
7	2 ⁵		
8	2 ⁶		
9	2 ⁷		
10	2 ⁸		
11	2 ⁹		
12	2 ¹⁰		
13	2 ¹¹		
14	2 ¹²		
15	2 ¹³		
16	2 ¹⁴		
17	2 ¹⁵		

Address & Data Input



On S1 Interface bd:

Observe Write Clocks at IC15 and adjust R1 for 600 ns between the first and fourth negative transitions.

Timing

Figure A-3

Function	Address			16-Bit Data Word			
	2^2	2^1	2^0	Mode bit 2^{15}	Range Char. $2^{14} 2^{13} 2^{12}$	3 BCD Digits Vernier $2^{11} \text{---} 2^0$	
Frequency	0	0	1	int/ext	Table D-2		
Delay	0	1	0	sgl/dbl	Table D-2		
Width	0	1	1	inv/norm	Table D-2		
Ldg Edge*	1	0	0	gate off/gate on	Table D-2		
Trig Edge*	1	0	1	not used	not used		
Offset	1	1	0	not used	0 1 0 = pos, 1 0 0 = neg		
Amplitude	1	1	1	neg/pos pulse pol	Attenuation Table D-2		

Function Address & Data Input

Function	Range Value	Range	Vernier
Frequency	0	0.5 Hz-4.995 Hz	100-999
	1	5 Hz-49.95 Hz	100-999
	2	50 Hz-499.5 Hz	100-999
	3	500 Hz-4.995 kHz	100-999
	4	5 kHz-49.95 kHz	100-999
	5	50 kHz-499.5 kHz	100-999
	6	500 kHz-4.995 MHz	100-999
Delay/Width	7	5 MHz-49.95 MHz	100-999
	0	10 ns-99.9 ns	100-999
	1	100 ns-999 μ s	100-999
	2	1 μ -9.99 μ s	100-999
	3	10 μ s-99.9 μ s	100-999
	4	100 μ s-999 μ s	100-999
	5	1 ms-9.99 ms	100-999
Ramp Rate	6	10 ms-99.9 ms	100-999
	7	100 ms-999 ms	100-999
	0	uncalibrated range*	100-999
	1	0.1-0.999 V/ns	100-999
	2	10.0-99.9 V/ μ s	100-999
Attenuation	3	1.0-9.99 V/ μ s	100-999
	4	0.1-0.999 V/ μ s	100-999
	5	10.0-99.9 V/ms	100-999
	0	(x 128) 40-80 mV	000-999
	1	(x 64) 80-156 mV	000-999
	2	(x 32) 156-312 mV	000-999
	3	(x 16) 312-625 mV	000-999
	4	(x 8) 0.62-1.25 V	000-999
	5	(x 4) 1.25-2.5 V	000-999
	6	(x 2) 2.5-5.0 V	000-999
	7	(x 1) 5.0-10.0 V	000-999

*The uncalibrated range gives minimum risetime (approx 3 ns) when 999 vernier is programmed. Intermediate values give risetimes from 3 ns and 30 ns, but programming is non-linear.

Table 1-2

Range Programming

JOB NO.	ASSEMBLIES REQ'D	COST CENTER	DATE

WHERE USED
1501A
1504

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B/M PAGE _____

ASSEMBLY NO. 350-21923

COPY DATE 3-28-78

E.C.O. 78-041

DESCRIPTION MOD KIT, OPT ISOL SERIAL BCD
3 ADDR/16 DATA, GND TRUE/POS TRUE

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	O.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A		ADD to INDEX							
B	*401-20666	3 Bit Isolated Address Bd	A309	1					
C	*401-21484	S1 Isolated Interface Bd	A308	1					
D	*401-22619	Serial D/A Board Assy	A305-307, A311-314	7					
E									
F		ADD to Rear Panel Assy							
G	*249-21385	Rear Subpanel Assy		1					
H									
I		ADD TO Standard Accessories							
J	146-26304	Documentation List	Prod Ref						
K	700-00034	Connector, 50 Pin Amphenol	P110-113	4					
L									
M									
N									
O									
P									
Q									
R									
S									
T									

NOTE: MARKETING OPTION 01-SØNI/SØPI
*SEE 1500 Series

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

WHERE USED 1500 Series	INDEX ☐	ASSEMBLY ☒	SPEC. ASSEM. ☐	B/M PAGE _____
	ASSEMBLY NO. <u>249-21385</u>			COPY DATE <u>4-17-73</u>
	DESCRIPTION <u>ASSEMBLY SUB-PANEL REAR</u>			E.C.O. _____

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

[illegible]

[illegible]

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

WHERE USED 1500 Series	INDEX ☐	ASSEMBLY ☒	SPEC. ASSEM. ☐	B/M PAGE _____
	ASSEMBLY NO. <u>401-20666</u>			COPY DATE _____
	DESCRIPTION <u>ISOLATED 3 BIT ADDRESS BOARD ASSEMBLY</u>			E.C.O. <u>76-050</u>

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	663-00124	Transistor 2N4401	Q1	1					
B									
C	665-00053	IC MC3000P	IC 5	1					
D	665-00123	IC MC4038P	IC 6	1					
E	665-00154	IC MC7242P	IC 2	1					
F	665-00210	LED HP 5082-4360	IC1, 3, 4, 7, 9	5					
G									
H	700-00144	Header, 3M 50 Pin 3433-2002	J1	1					
I									
J									
K									
L									
M									
N									
O									
P									
Q									
R									
S									
T									

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

WHERE USED
1500 Series

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ASSEMBLY ☐

SPEC. ASSEM. ☐

B/M PAGE

COPY DATE

E.C.O.75-138

ASSEMBLY NO. 401-21484

DESCRIPTION S-1 INTERFACE ISOLATED BOARD ASSEMBLY

FILLED BY DATE RELEASED TO DATE

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	400-21483	PC Board		1					
B	401-21484	Assembly Drawing	Prod Ref						
C	140-21485	Schematic	Prod Ref						
D									
E	311-00007	Cap, Cerm 100pf 1KV 10%	C9,10	2					
F	311-00009	Cap, Cerm 500pf 1KV 10%	C8,11	2					
G	311-00035	Cap, Cerm 15pf 1KV 10%	C7	1					
H	311-00041	Cap, Cerm .1 μ f 12V	C1	1					
I	311-00074	Cap, Cerm .01 μ f 100V	C3-6 12-15	8					
J	318-00005	Cap, Tant 10 μ f/20V	C2	1					
K									
L	335-00022	Choke 1 μ h	L1	1					
M									
N	376-00022	Diode, 1N914B	CR1	1					
O									
P	551-00041	Potentiometer 5K 89PR	R1	1					
Q									
R	595-00101	Resistor 100 Ω $\frac{1}{2}$ W 5%	R25,28	2					
S	595-00102	Resistor 1K $\frac{1}{2}$ W 5%	R18-22,45	6					
T	595-00152	Resistor 1.5K $\frac{1}{2}$ W 5%	R27	1					

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

WHERE USED
1500 Series

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ASSEMBLY ☒
SPEC. ASSEM. ☐

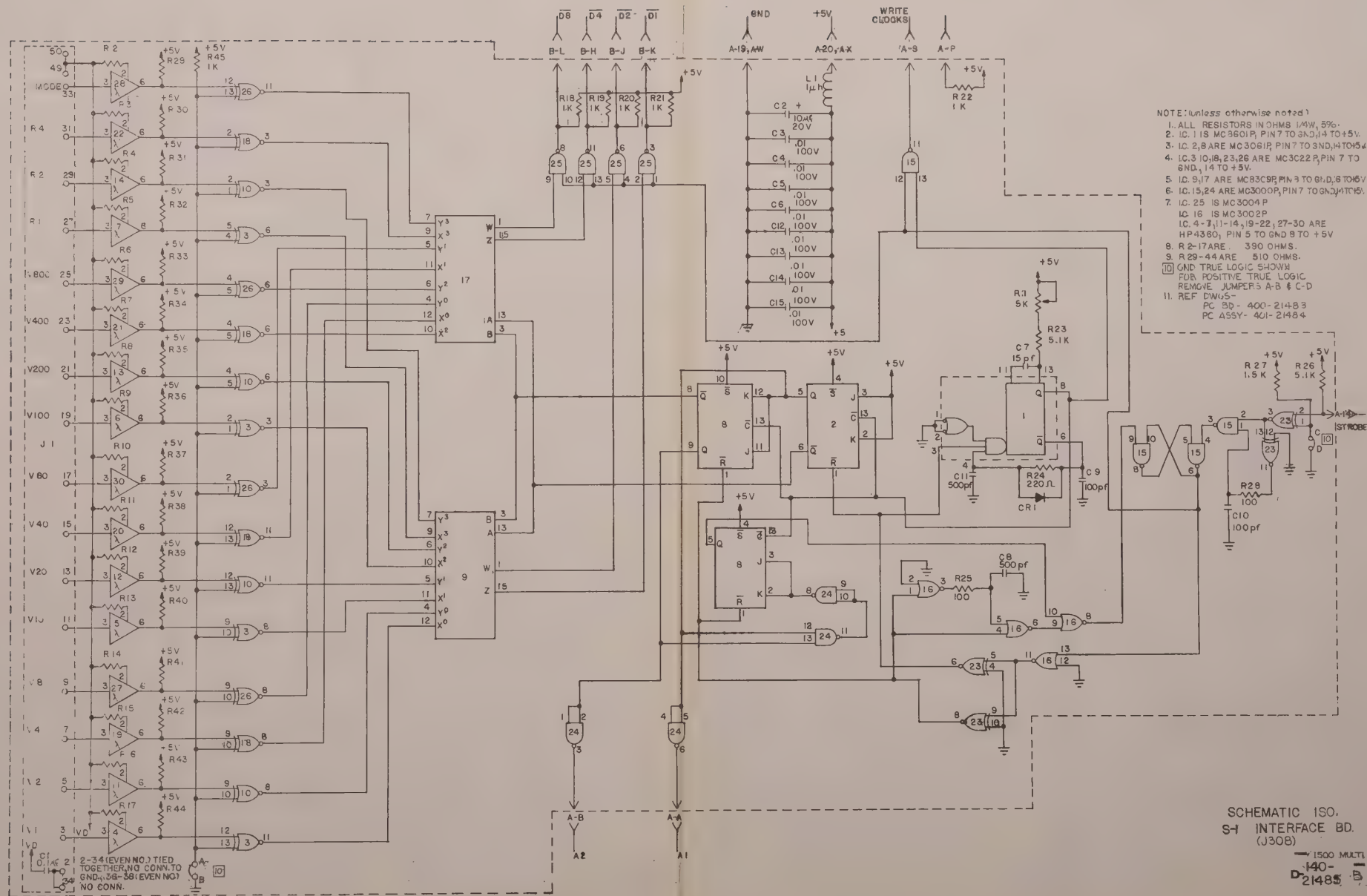
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COPY DATE _____
E.C.O. _____

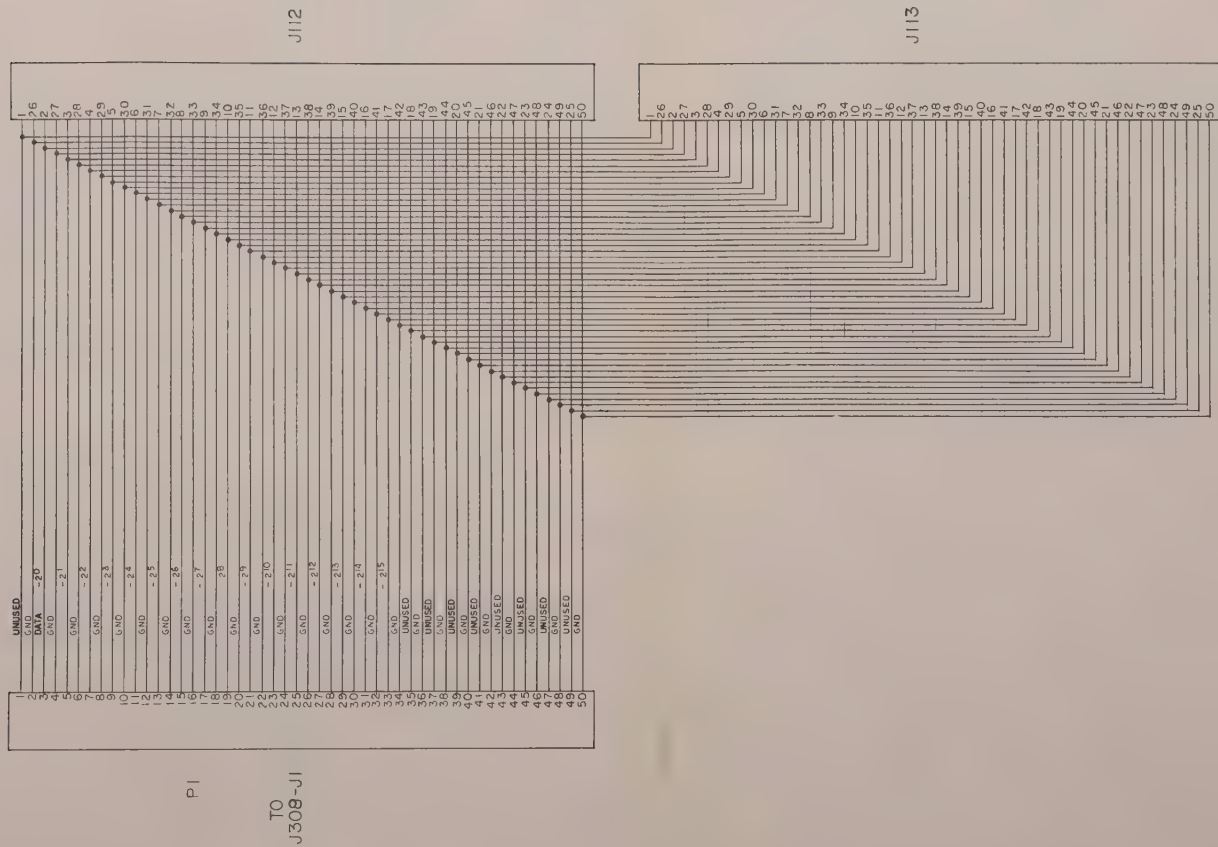
ASSEMBLY NO. 401-21484

DESCRIPTION S-1 INTERFACE ISOLATED BOARD ASSEMBLY

FILLED BY _____
DATE _____
RELEASED TO _____
DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	595-00221	Resistor 220Ω ¼W 5%	R24	1					
B	595-00391	Resistor 390Ω ¼W 5%	R2-17	16					
C	595-00512	Resistor 5.1K ¼W 5%	R23,26	2					
D	595-00511	Resistor 510Ω ¼W 5%	R29-44	16					
E									
F	665-00053	IC MC3000P	IC 15,24	2					
G	665-00078	IC MC3004P	IC 25	1					
H	665-00084	IC MC3022P	IC3,10,18 23,26	5					
I	665-00130	IC MC8601P	IC 1	1					
J	665-00110	IC MC3002	IC 16	1					
K	665-00054	IC MC3061P	IC 2,8	2					
L	665-00145	IC MC8309P	IC9,17	2					
M	665-00210	LED, HP 5082-4360	IC4-7,11- 14,19-22						
N			27-30	16					
O									
P	700-00144	Header, 50 Pin, 3M	J1	1					
Q									
R									
S									
T									





PI
TO
J308-J1

SCHEMATIC, 16 BIT
DATA BUSS

OPTION 01 SON
SERIAL BY 16-BIT WORD PROGRAMMING

The 16-bit serial by word option is designed for systems which incorporate a party-line data bus system where address and data are on separate lines. Data which was previously written in may be read out. This option also provides signals that can be used in request-answer closed loop systems.

A data input word must always be 16 bits, one word per function. The data word contains one bit for mode control, three bits for range selection, and 12 bits for three digits of vernier control.

The function address code and the 16-bit data word are defined in Table A3-1. Table A3-2 gives the range values and the decimal range number. As an example, for a frequency of 260 kHz, Internal Clock:

$2^2 \ 2^1 \ 2^0$
 ADDRESS - X X X 0 0 1
 $2^{15} \quad \quad \quad 2^{11} \quad \quad \quad 2^7 \quad \quad \quad 2^3 \quad \quad \quad 2^0$
 DATA - 0 / 1 0 1 / 0 1 0 1 / 0 0 1 0 / 0 0 0 0

When writing in data, the address, data and write line must be valid for 100 ns, minimum, before the Strobe, and must remain valid for 0.9 μ s after the Strobe.

When reading out data, the address and read lines must be valid for 100 ns minimum before the Strobe and remain valid for 0.9 μ s after the Strobe. The internal data will become valid on the data lines 0.8 μ s after the Strobe and remain valid for 0 μ s. The length of time the data is valid may be changed by adjusting the time constant R17-C1 shown on schematic diagram 140-22172. The time constant R15-C2 must also be changed if the FIN signal is used and it is desired to have the FIN signal occur near the end of the time that the data is valid.

If the Write or Read line goes false too soon, only partial data will be written in, and no data will be read out.

II RESET MODES

When primary power is turned on, all internal storage is reset to zero, and the Model 1501A is in the following modes: maximum attenuation, inverted pulse mode, negative pulse, zero offset, Gate Off mode, frequency, delay, width, rise and fall times at minimum, internal clock, and single pulse. After initial programming, reset of internal storage can be done in two ways:

- 1) When eight lines are used for the address, a binary 255 address, a Write command, and a Strobe resets all registers to zero. This may be inhibited with an internal strap to ground; S4, shown on schematic diagram 140-22175.
- 2) One of the following, selected by wire straps on Address Board, S5, schematic diagram 140-22175.
 - a) Instrument address with the three least significant bits zero, and a Strobe.
 - b) Single external Master Reset line pulled to ground. The logic levels for the Master Reset are TTL-compatible (0 to +5 V).

Master Reset, BIZ, and FIN signals are always ground true. The Strobe, Read, Write, Address, and Data inputs can be selected for positive true or ground true.

III ADDRESS (Refer to schematic diagram 140-22175)

Each bit is selected individually by switches S1 and S2 mounted on the Address Board. For ground true logic, switches S1-a, S1-b, and S1-c must be closed to ground. The other switches will be closed or open if a bit is "1" or "0" respectively. For positive true logic, the switch positions are reversed.

If reset on address 255 is used, switch S3 is strapped to ground for ground true logic, or left open for positive true logic. If it is desired to inhibit reset on address 255, switch S4 is strapped to ground.

IV DATA LOGIC POLARITY (Refer to schematic diagram 140-22172)

All data bits for input data are selected by grounding S1 for ground true data or leaving S1 open for positive true data.

Ground true output data is selected by leaving S2 open. For positive true output data, S2 is strapped to ground. It should be noted that output data is from open collector NPN transistors and is valid only during the time indicated in the timing diagram. It should also be noted that there are no pull-up resistors in the data input/output lines.

V STROBE, READ, WRITE LOGIC POLARITY (Refer to schematic diagram 140-22172)

These three signals must have the logic true levels, and are set by switch S3. If S3 is set to ground, the levels are ground true, and if left open, the levels are positive true.

VI SIGNAL INPUT LOADING

A low level (ground) is equal to or less than 0.5 V. A high level is +2.5 V minimum to +5 V maximum. A low level must not go more than 0.5 V below ground.

Address and data bits have a maximum loading in the high state of 250 μ A.

Strobe, Read, and Write are each one TTL load plus 5.1K resistor to +5 V.

When the master reset line is used, it is two TTL loads plus a 1K resistor to +5 V.

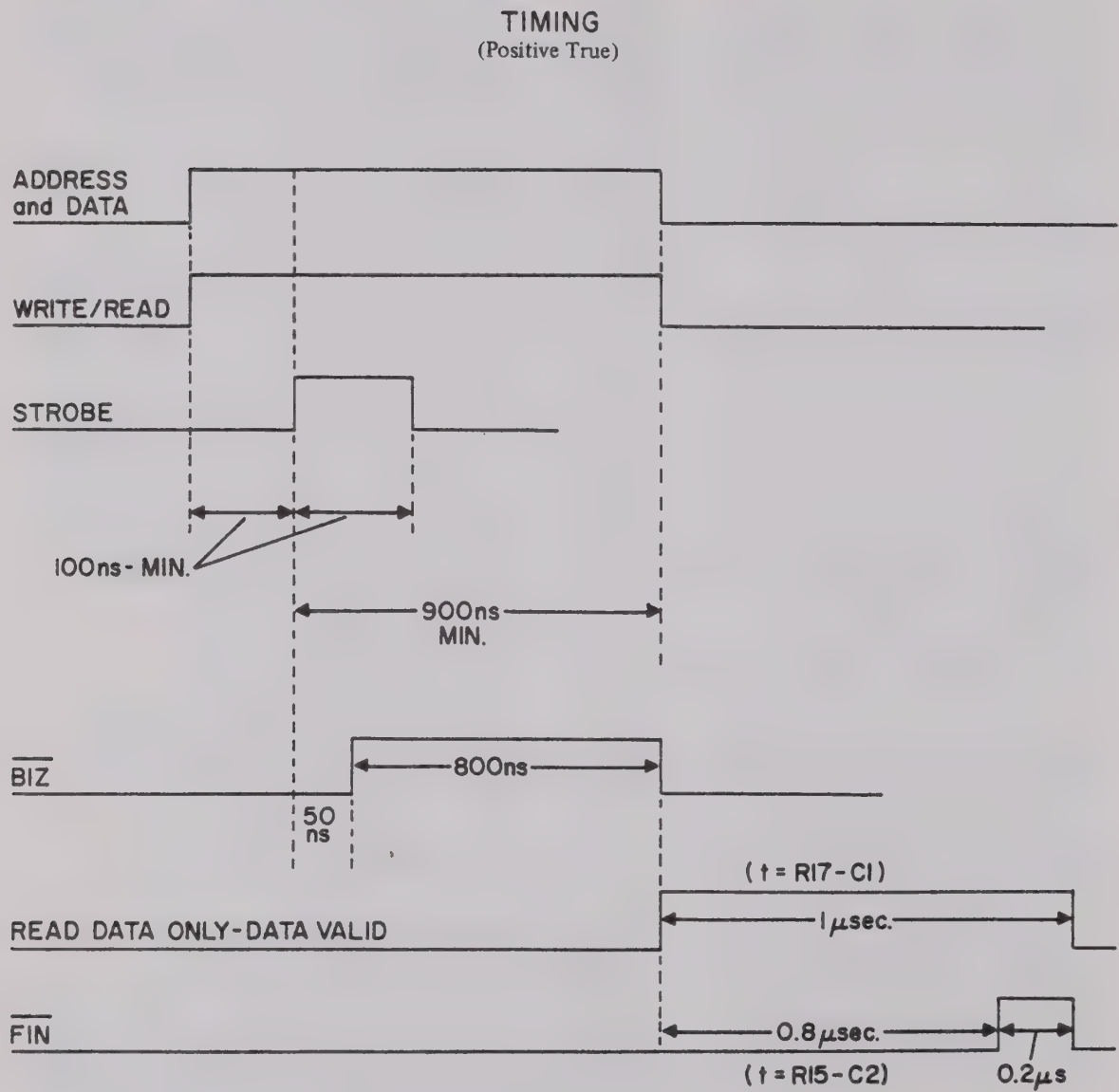
VII SIGNAL INPUT CONNECTIONS

Address Data connections are listed in Table A3-3.

VIII SERIAL BY WORD INTERFACE CIRCUIT DESCRIPTION

- a. Address Card J309A (Refer to Schematic 140-22175)

Figure A3-0 Timing Diagram



- (1) General. The address lines are buffered by IC's 3, 6, 8, and 10. These are 2 input positive AND gates. They present a maximum D.C. load of 250 μ A when their input is in the high state.

The output from these IC's go to exclusive NOR gates for true logic level selection. These gates are IC's 2, 5, 7, and 9. Their output is always high state true.

The three least significant bits are decoded by IC 13, a 1-of-8 decoder. The output from IC 13 is ground true and is enabled via pin 7 when the rest of the address bits are true. The exclusive NOR gates are open-collector so that any one being in the low state holds pin 7 of IC 13 low, which inhibits any of the address lines from going low.

When a proper address is decoded, pin 7 of IC 13 is pulled high and also pin 9 of IC 12. IC 12-pin 8 then goes low which allows a strobe pulse to start a read or write sequence.

- (2) Reset Modes. IC 1 and IC 4 are connected to decode the binary address 255. The three least significant bits are gated with the write signal so that, with a strobe pulse to pin 2 of IC 11, a reset signal is generated. S-3 is strapped to ground if the address input is ground-true logic. S-4 is strapped to ground if address 255 is not used as a system reset.

The three least significant bits, decoded by IC-13 can also be used as a reset signal by connecting pin 3 of IC 13 to pin 2 of IC 12. This causes pin 3 of IC 12 to go positive so that a strobe pulse on pin 2 of IC 11 will generate a reset pulse.

An external Master Reset line is provided on pin 1 of the connector. This line is activated in the low state. To use this reset mode, connect S-5 between pin 1 of IC 11 and pin 2 of IC 12. This will then produce a reset pulse from IC 11 independent of any other input signals.

The power-on reset is generated by C1 holding down pin 4 of IC 12. Pin 6 is forced to a high state which turns on Q1 long enough for all power supplies to attain their steady-state operating values.

The width of the reset pulse is determined by C3 and R24. This width should be greater than 80 ns. With the component values shown, the width at pin 6 of IC 11 will be 100 ns +20 ns. The width at pin T of the circuit board will in general be much wider, due to the storage time of Q1.

- b. Data Card (Refer to Schematic 140-22172). The data logic provides the control for the flow of data to the storage registers in groups of four bits when writing into the instrument, and constructing a 16-bit parallel word when reading the data stored in the instrument.

The read, write, and strobe signals go through exclusive NOR gates in IC 25 for logic true level selection.

In order to do a write sequence, the address and data lines, and the write signal should be allowed to settle for a minimum of 100 ns, before a strobe is sent to the interface. The write signal, being high at the output of IC 25, pin 3, causes pin 5 of IC 1 to be low and therefore inhibit the read sequence. The read line should be low so pin 9 of IC 1 is high. With a valid address being low, a strobe pulse is differentiated through IC 13, pin 1, and IC 2, pins 12 and 13. (See Figure A3-2, part 1.) The output from IC 2, pin 11, will be a negative-going spike, which forces pin 6, IC 2 high. IC 1 pin 12 goes high, and because all the inputs to that gate are high at this time, the output, pin 8, IC 1 goes low. This initiates the write sequence.

At the time of the negative spike on IC 2 pin 11, pin 10 of IC 2 is high so pin 8 of IC 2 will go negative thus holding pin 6, IC 2 positive.

When IC 1, pin 8 goes negative, IC 4, pin 6 goes positive, removing the reset on the binaries IC 28, and IC 16, and allowing the multivibrator, IC 3, to start running, via pin 3, IC 3. IC 1, pin 8, also allows write clocks to pass through IC 13, pin 10, and gates the input data through IC 18.

The two binaries of IC 28 select four bits at a time via the data selectors IC 6 and IC 7. They also select the proper four bits of storage on the D/A cards via the address lines from IC 26, pin 8 and 11.

The write sequence is terminated when pins 5 and 9 of IC 28 are both high, presenting a high input to binary IC 16. This high input causes this binary to be set. Pin 5 of IC 16 goes high, forcing pin 11 of IC 13 low which then resets the input flip-flop, pins 6 and 8 of IC 2. IC 4, pin 6 goes low, turning off the multivibrator, IC 3, and resets the binaries, IC 16 and IC 28.

The write clocks at pin A-S, are negative going. (See Figure A3-2, part 2.) The first character, 4 bits, of data, is strobed into the registers on the negative going edge. When this clock waveform goes positive, the address binaries of IC 28, change state. The next character is then gated onto the common data lines D1, D2, D4, and D8.

- (1) Multivibrator Timing. The quiescent state of the multivibrator, IC 3, is with pin 8 low, and pin 6 high. Pin 4 will also be high, being connected to pin 6 via R10. When pin 3 goes high, pin 8 goes high, and the timing state (determined by C6 and R19 and R20) is started. Pin 6 goes low and discharges C5 through the diode. At the end of the timing state, pin 6 goes high and pin 4 goes high after a time determined by C5 and R10, and the input threshold of the IC. This delays the start of the next timing state to allow settling time of the address and data.

R20 should be adjusted by observing the wave form either at pin 3 of IC 14, or pin A-S. Adjust R20 so that the time between the first negative-going edge and the fourth negative-going edge is 0.6 μ sec. The time that the wave form is at the high level is determined by C5 and R10, and should be 80 ns to 100 ns.

During a normal cycle, the clock waveform should return to the high level approximately 100 ns after the fourth negative transition.

- (2) Read Sequence. With the read line in the true state, pin 4 of IC 1 will be high so that when pin 6 of IC 2 goes high with a strobe, pin 6 of IC 1 will go low, initiating a Read cycle.

As in a write cycle, the multivibrator is started and binaries IC 28 address the characters. With the address lines on A-A and A-B, the function address line from the address card, and the read signal on pin A-P, the characters are strobed 4 bits at a time, into the D flip-flops in IC's 19, 20, 31, and 32. The strobes to the D flip-flops are routed by IC-29 and address binaries, IC 28. The first strobe goes to IC 32, the second to IC 31, third to IC 20, and the fourth to IC 19. The characters are thus set up in the same order as when they are written in, most significant bits first, i.e., Mode bit and Range bits first.

The data at the inputs to gates IC 30 is ground true. For ground true data out, S 2 must be open so that pins 1, 5, 13, and 10 are high.

Table A3-1 Function Address and Data Input

Function	Address	16-Bit Data Word			
	X X 3 dependent bits	Mode bit	Range Char.		3 BCD Digits Vernier
	2 ² 2 ¹ 2 ⁰	2 ¹⁵	2 ¹⁵ 2 ¹⁴ 2 ¹³ 2 ¹²	2 ¹¹ ---- 2 ⁰	
Frequency	X X 0 0 1	0/1 int/ext	Table B-2		
Delay	X X 0 1 0	sgl/dbl	Table B-2		
Width	X X 0 1 1	inv/norm	Table B-2		
Ldg Edge	X X 1 0 0	norm/gate on	Table B-2		
Trlg Edge	X X 1 0 1	not used	not used		
Offset	X X 1 1 0	not used	0 1 0 = pos 1 0 0 = neg		
Amplitude	X X 1 1 1	neg/pos pulse pol	Attenuation Table B-2		

Table A3-2 Range Programming

Function	Range Value	Range	Vernier
Frequency	0	0.5 Hz-4.995 Hz	100-999
	1	5 Hz-49.95 Hz	100-999
	2	50 Hz-499.5 Hz	100-999
	3	500 Hz-4.995 kHz	100-999
	4	5 kHz-49.95 kHz	100-999
	5	50 kHz-499.5 kHz	100-999
	6	500 kHz-4.995 MHz	100-999
	7	5 MHz-49.95 MHz	100-999
Delay/Width	0	10 ns-99.9 ns	100-999
	1	100 ns-999 ns	100-999
	2	1 μ s-9.99 μ s	100-999
	3	10 μ s-99.9 μ s	100-999
	4	100 μ s-999 μ s	100-999
	5	1 ms-9.99 ms	100-999
	6	10 ms-99.9 ms	100-999
	7	100 ms-999 ms	100-999
Ramp Rate	0	uncalibrated range*	100-999
	1	0.1-0.999 V/ns	100-999
	2	10.0-99.9 V/ μ s	100-999
	3	.0-9.99 V/ μ s	100-999
	4	0.1-0.999 V/ μ s	100-999
	5	10.0-99.9 V/ms	100-999
Attenuation	0	(x 128) 40-80 mV	000-999
	1	(x 64) 80-156 mV	000-999
	2	(x 32) 156-312 mV	000-999
	3	(x 16) 312-625 mV	000-999
	4	(x 8) 0.62-1.25 V	000-999
	5	(x 4) 1.25-2.5 V	000-999
	6	(x 2) 2.5-5.0 V	000-999
	7	(x 1) 5.0-10.0 V	000-999

*The uncalibrated range gives minimum risetime (approx 3 ns) when 999 vernier is programmed. Intermediate values give risetimes from 3 ns and 30 ns, but programming is non-linear.

Table A3-3 Data and Address Input/Output

ADDRESS - J110 and J111

Pin	Signal	Pin	Signal
1	Master Reset	14	2 ¹²
2	2 ⁰	15	2 ¹³
3	2 ¹	16	2 ¹⁴
4	2 ²	17	2 ¹⁵
5	2 ³	18	not used
6	2 ⁴	19	Strobe
7	2 ⁵	20	BIZ
8	2 ⁶	21	FIN
9	2 ⁷	22	not used
10	2 ⁸	23	WRITE
11	2 ⁹	24	READ
12	2 ¹⁰	25	not used
13	2 ¹¹	26-50	ground

DATA - J112 and J113

Pin	Signal	Pin	Signal
1	not used	8	2 ⁶
2	2 ⁰	9	2 ⁷
3	2 ¹	10	2 ⁸
4	2 ²	11	2 ⁹
5	2 ³	12	2 ¹⁰
6	2 ⁴	13	2 ¹¹
7	2 ⁵	14	2 ¹²
15	2 ¹³	26-50	ground
16	2 ¹⁴		
17	2 ¹⁵		
18-25	not used		

Rear-Panel Input/Output Connections (All Type BNC)

Ext Drive In	J105
Trigger Out	J103
Async. Gate In	J106
Sync. Gate In	J107
Pulse Output	J108

NOTE

Analog Control connector J109 is not used in Model 1501A's with serial by 16-bit word programming.

When the read sequence ends, IC 16, pin 6 goes momentarily low which trigger the two one-shots, IC-15. The output, pin 13, of IC 15 goes high forcing pin 8 of IC 4 low, which gates the 16 bits of data onto the data buss via IC's 34 thru 40. These are open collector power gates, which are in the low state with both inputs low.

Note that during a write cycle, pin 8 of IC4 will not go low because pin 6 of IC5 will not be high. Pin 6 is high during a read cycle via pin 6 of IC1, and pins 8 and 11 of IC5, C4 and R13 ensure that pin 4 of IC5 is low when pin 13 of IC4 goes high at the end of the Read cycle.

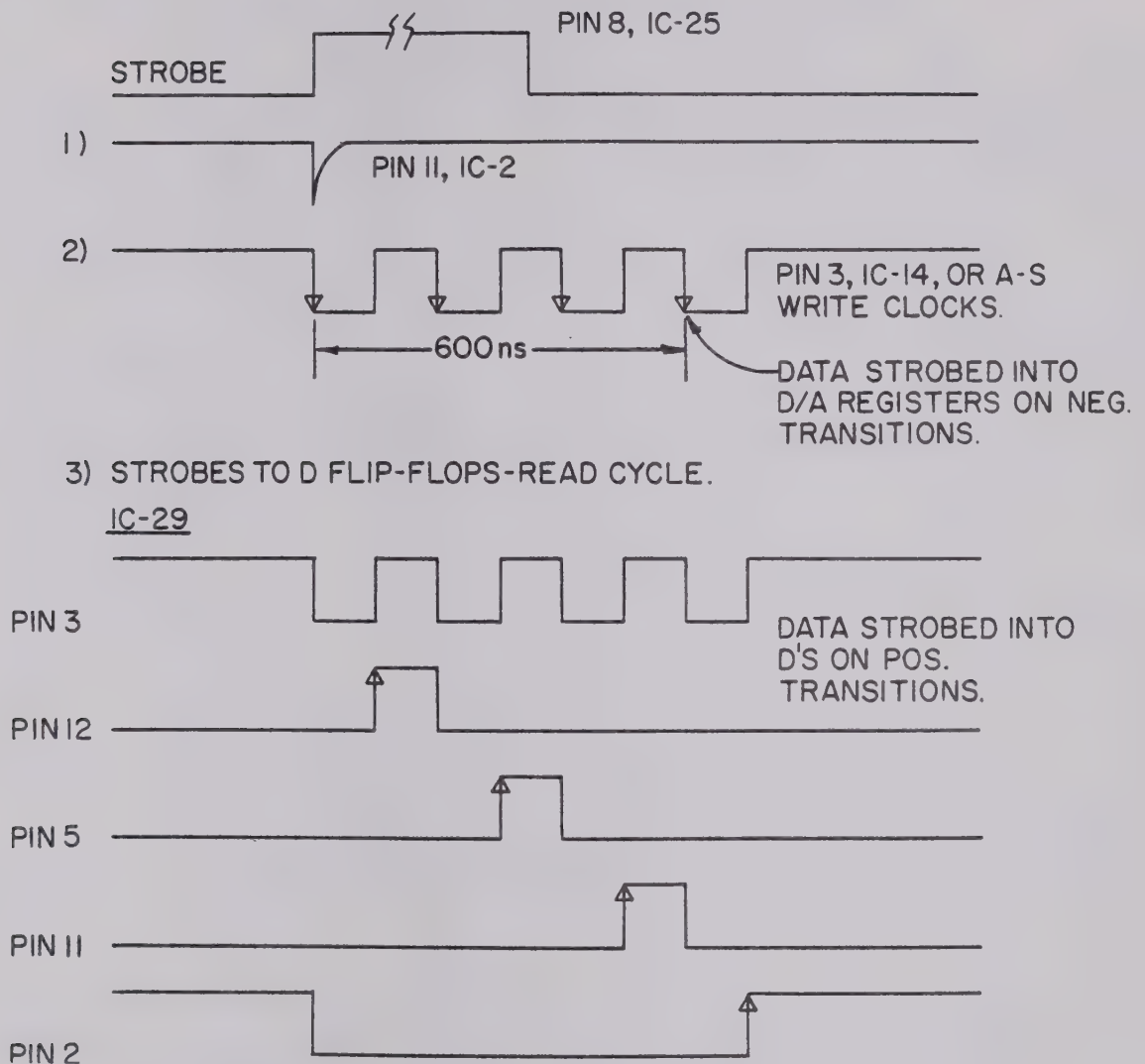
The readout data is valid for the timing state at pin 13 of IC15. This is normally set for 1 use, but may be set for any time required.

The FIN signal is low state true, and begins at the trailing edge of pin 12, IC15, and ends at the trailing edge of pin 4, IC15.

As indicated above, the strobes to the D flip-flops of IC's, 19, 20, 31, and 32 are distributed through IC29. The proper waveforms during a Read cycle are shown on Figure A3-2, part 3.

If the write or read line goes false before the end of a cycle, pin 6, IC4 will go negative and be differentiated through pin 5, IC13, and pins 9 and 10, IC12. This causes pin 11 of IC13 to go negative which then ends the cycle. If this occurs, only partial data is written in, and no data will be gated out.

Figure A3-4 Waveforms-Schematic 140-22172



JOB NO.	ASSEMBLIES REQ'D	COST CENTER	DATE

WHERE USED

1501A

1504

INDEX ☒

ASSEMBLY ☐

SPEC. ASSEM. ☐

B/M PAGE _____

ASSEMBLY NO. 350-21921

COPY DATE 3-28-78

E.C.O. 78-041

DESCRIPTION MOD KIT, SERIAL (BCD), 16 ADDR,
16 DATA, GND TRUE/POS TRUE

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A		ADD to INDEX							
B	*401-22171	S1 Interface Bd Assy	A308	1					
C	*401-22174	16 Bit Address Bd Assy	A309	1					
D	*401-22619	Serial D/A Board Assy	A305-307, A311-314	7					
E									
F		ADD to Rear Panel Assy							
G	*249-21385	Rear Subpanel Assy		1					
H									
I		ADD to Standard Accessories							
J	146-26303	Documentation List	Prod Ref						
K	700-00034	Connector, 50 Pin Amphenol	P111-113	4					
L									
M									
N									
O									
P									
Q									
R									
S									
T									

NOTE: MARKETING OPTION 01-SØN/SØP
*SEE 1500 Series

WHERE USED 1500 Series	INDEX ☐	ASSEMBLY ☒	SPEC. ASSEM. ☐	B/M PAGE _____
	ASSEMBLY NO. <u>401-22174</u>			COPY DATE _____
	DESCRIPTION <u>16 BIT ADDRESS BOARD ASSEMBLY</u>			E.C.O. 77-033
	ED BY _____	DATE _____	RELEASED TO _____	DATE _____

[illegible]

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

WHERE USED
1500 Series

INDEX ☐

ASSEMBLY ☒

SPEC. ASSEM. ☐

B/M PAGE _____

ASSEMBLY NO. 401-22174

COPY DATE _____

E.C.O. 77-033

DESCRIPTION 16 BIT ADDRESS BOARD ASSEMBLY

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	400-22173	PC Board		1					
B	401-22174	Assembly Drawing	Prod Ref						
C	140-22175	Schematic	Prod Ref						
D									
E	311-00041	Cap, Cerm .1 μ f 12V	C4	1					
F	311-00003	Cap, Cerm 25pf	C3	1					
G	318-00005	Cap, Tant 10 μ f 20V	C2	1					
H	318-00019	Cap, Tant 47 μ f 20V	C1	1					
I									
J	335-00022	Choke 1 μ h	L1	1					
K									
L	376-00022	Diode, 1N914B	CR1	1					
M									
N	595-00102	Resistor 1K $\frac{1}{4}$ W 5%	R19-23 27-35	14					
O	595-00103	Resistor 10K $\frac{1}{4}$ W 5%	R25,37	2					
P	595-00331	Resistor 330 Ω $\frac{1}{4}$ W 5%	R17,26,36	3					
Q	595-00511	Resistor 510 Ω $\frac{1}{4}$ W 5%	R18	1					
R	595-00512	Resistor 5.1K $\frac{1}{4}$ W 5%	R1-16,24	17					
S	624-00061	Header	S1,2	2					
T	624-00060	Switch, D.I.P, 8 Position	S1, 2	2					

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

WHERE USED
1500 Series

1501A-21
1501A-22

INDEX ☐ ASSEMBLY ☒ SPEC. ASSEM. ☐
ASSEMBLY NO. 401-22171
DESCRIPTION S-1 INTERFACE BOARD ASSEMBLY

B/M PAGE
COPY DATE
E.C.O.
77-033

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	400-22170	PC Board		1					
B	401-22171	Assembly Drawing	Prod Ref						
C	140-22172	Schematic	Prod Ref						
D									
E	311-00002	Cap, Cerm 20pf 1KV 10%	C6	1					
F	311-00006	Cap, Cerm 50pf 1KV 10%	C1,2	2					
G	311-00007	Cap, Cerm 100pf 1KV 10%	C4,7,13	3					
H	311-00009	Cap, Cerm 500pf 1KV 10%	C3,5	2					
I	311-00074	Cap, Cerm, .01μf 100V	C9-12	4					
J	318-00005	Cap, Tant 10μf 20V	C8	1					
K	335-00022	Choke, 1μh	L1	1					
L	376-00022	Diode, 1N914B	CR1	1					
M									
N	551-00041	Potentiometer 5K 89PR	R20	1					
O	551-00055	Potentiometer 50K 89PR	R15,17	2					
P	595-00101	Resistor 100Ω ½W 5%	R13,14,21	3					
Q	595-00102	Resistor 1K ½W 5%	R1-6,9	7					
R	595-00221	Resistor 220Ω ½W 5%	R10	1					
S	595-00472	Resistor 4.7K ½W 5%	R16,18	2					
T	595-00512	Resistor 5.1K ½W 5%	R19,22-25	5					

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

WHERE USED
1500 Series

INDEX ☐

ASSEMBLY ☒

SPEC. ASSEM. ☐

B/M PAGE _____

COPY DATE _____

E.C.O. 78-048

1501A-21

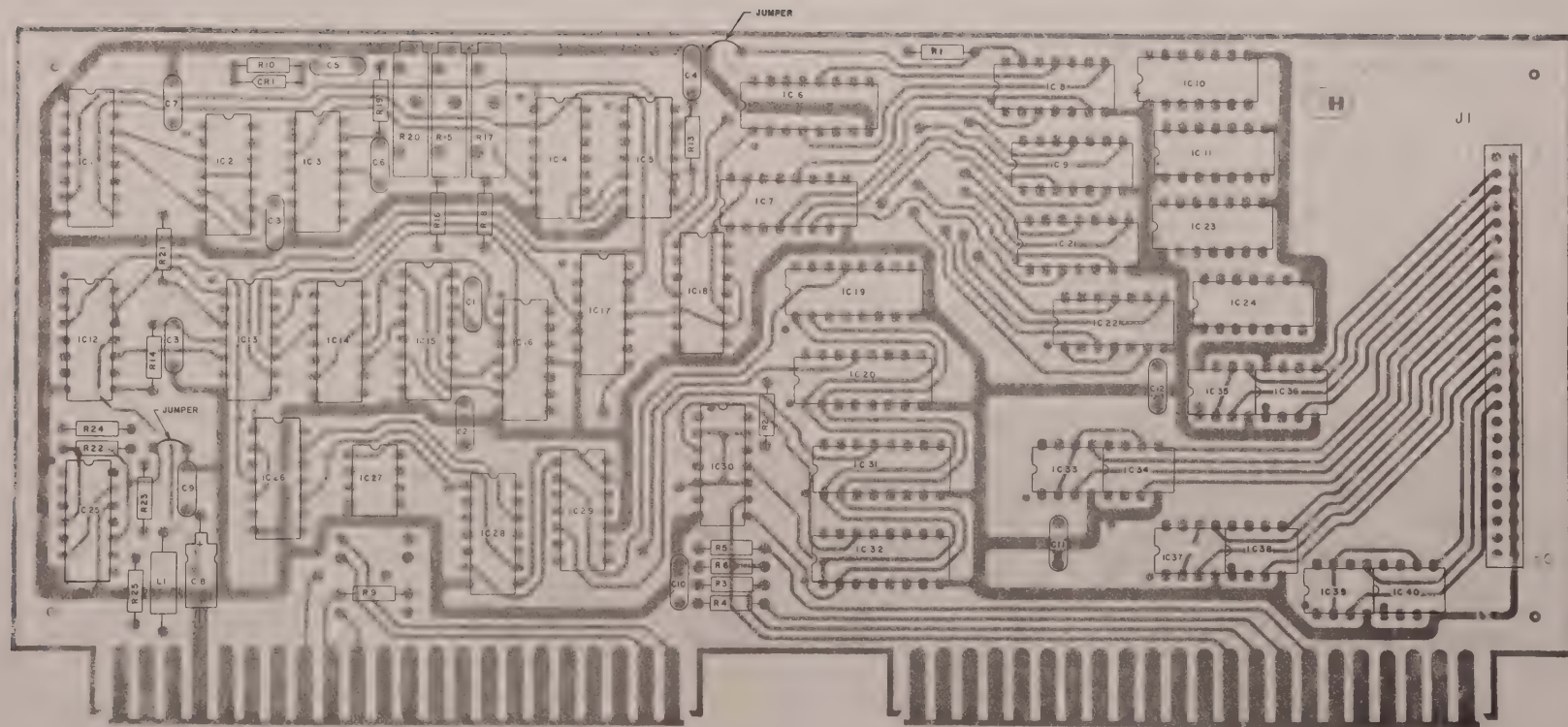
1501A-22

ASSEMBLY NO. 401-22171

DESCRIPTION S-1 INTERFACE BOARD ASSEMBLY

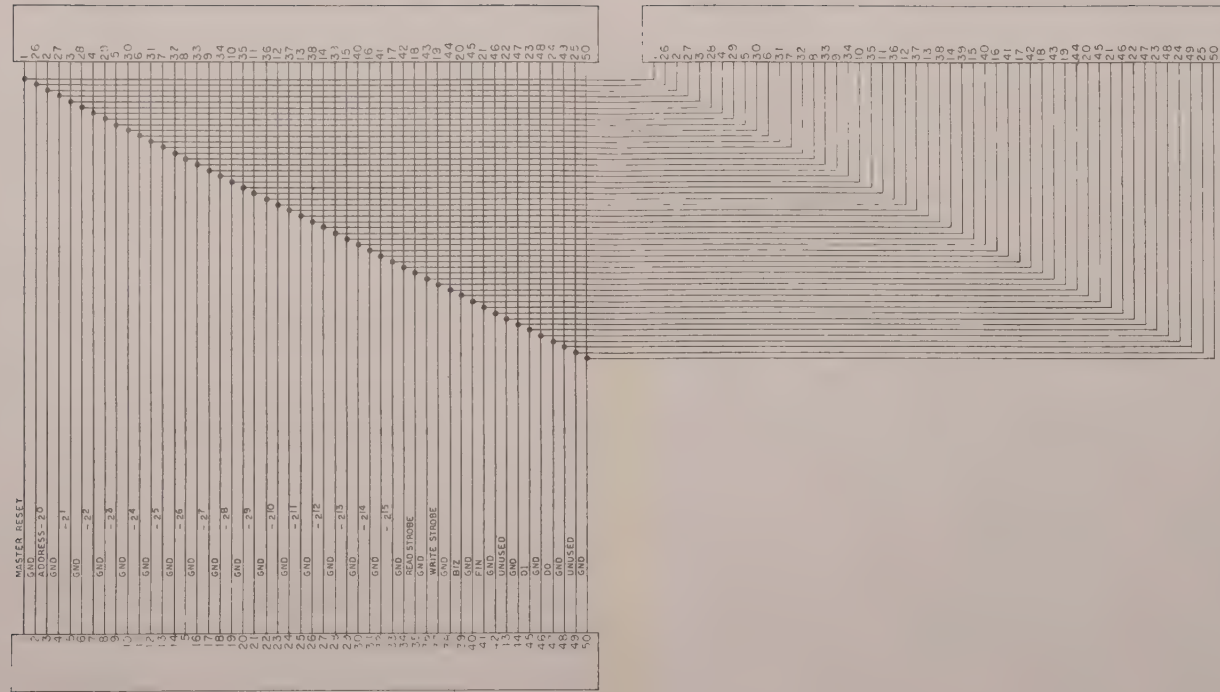
FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	665-00053	IC MC 3000P	IC2,5,12, 14,26	5					
B	665-00054	IC MC 3061P	IC 16,28	2					
C	665-00078	IC MC 3004P	IC 18	1					
D	665-00084	IC MC 3022P	IC8,9,21, 22,25,30	6					
E	665-00100	IC SN75453P	IC33-40	8					
F	665-00110	IC MC 3002P	IC 13,17	2					
G	665-00144	IC MC 4015P	IC19,20, 31,32	4					
H	665-00130	IC MC8601P	IC 3	1					
I	665-00133	IC SN75452P	IC 27	1					
J	665-00134	IC SP384A	IC10,11, 23,24	4					
K	665-00139	IC SN74123N	IC 15	1					
L	665-00146	IC MC 3024P	IC 1,4	2					
M	665-00151	IC MC 4002 P	IC 29	1					
N	665-00145	IC MC8309P	IC 6,7	2					
O									
P	700-00283	Connector, 50 Pin Berg -	J1	1					
Q									
R									
S									
T									



ASSEMBLY DRAWING
S-I INTERFACE BOARD

MODEL: 1501 A
401-
D-22171 C



APPENDIX A-4

OPTION 01 AON ASCII PROGRAMMING

I INTRODUCTION

The ASCII programming option is designed to operate in a party-line data transfer bus. The address and data, both to and from the Model 1501A, are transmitted over the same seven lines (eight lines with parity check). The code used is standard ASCII alphanumeric.

When desired, each character can be checked for even parity. When a parity error is detected, an error signal is generated by the Model 1501A and the character having the parity error is inhibited from entry into the internal storage registers. When data is read from the Model 1501A, even parity is generated, character by character, and the proper parity bit is present on the eighth ASCII data line.

When reading program data from the Model 1501A, the clock may be supplied externally, or an internal clock may be selected by a jumper on one of the internal programming circuit boards.

The ASCII programming option can be operated with the E-H Model 1012 Keyboard, provided external +5 V power is supplied, and the clock output is shifted from pin 20 to pin 18 on the programming connector.

II PROGRAMMING FORMAT

- a. Address. There are two basic address requirements; unique instrument address, and function address within the instrument. The instrument must be addressed before any programming or interrogation of the unit can be done. The address consists of three characters, alpha or numeric, and are selected by jumpers on the internal address board. Unless otherwise specified, the instruments are factory-wired with an address "PG1". If desired, this can be changed by changing the jumpers on the address board. For example, if "PG2" is desired, the connection at IC11 pin 2 should be moved from the A1 line to the A2 line. Once the address characters have been entered, the instrument functions are available for programming or readout. The instrument address, once entered, remains valid until a period "." is entered. At this point, no further programming or program readout can be done until the instrument is once again addressed.

Once the instrument address has entered, a single alpha character selects a function such as frequency,

delay, amplitude, offset, etc. These function characters are listed in Table A4-1. The next five numeric characters following the function address are stored as data for the function. The sequence and definition of the five data characters are also shown in Table A4-1.

- b. **Stored Data Readout.** Stored program data may be read out, one complete function at a time, by first addressing the instrument, then selecting the function with a single alpha character. The next character following the function character must be a question mark "?". When the "?" has been clocked in, the first data character will be present on the data input/output lines. There must be five clock pulses sent to the instrument for a complete readout of the five data characters. Once a readout is initiated, all five characters must be clocked out. A period will not reset the box address once a readout has initiated. Characters are read out in the same sequence as written (see Table A4-1).
- c. **Data Reset.** When primary power is applied to the Model 1501A (turning on the POWER switch), all internal storage registers are reset to "0" automatically. This means that initially all functions must be programmed on the initial process after power turn-on, ti can be edited independently. In operation, complete data reset can occur in two ways.
 - 1) **CO.** This reset mode is used in the following manner: The instrument address is entered on the data lines, followed by "CO". This resets all function storage registers to zero, but does not reset the instrument address.
 - 2) **EXTERNAL RESET (GOMR).** This is a single external control line which, when activated, resets all functions as well as the instrument address. This line is brought out to pin 22 of rear-panel connector J109.

In the reset state, functions are programmed as follows: maximum attenuation, inverted pulse mode, negative pulse, zero offset, Gate Off mode, frequency, delay, width, rise and fall times at minimum, internal clock, and single pulse.

III DATA FORMAT

Referring to Table A4-1, the Function column lists the seven function together with their proper alpha characters. The first character following the function character is mode control

character. For example, the mode control character for frequency, selects either internal or external clock by entry of a "0" or a "1", respectively. Only the least significant bit of the character is stored, so that any even number will be recognized as a "0" and any odd number will be recognized as a "1".

The mode characters for "T", positive ramp, and "0", offset are not used and may be any numeric character. There must, however, be a character entered (usually zero) when the function is programmed.

Following the mode character is a range character, selected by referring to Table A4-1. In the case of offset, a 2 selects positive offset and a 4 selects negative offset. The "T" (positive ramp) function does not use a range character, but the position must be filled with numeric character, as in the "T" and "0" mode functions described previously.

The third, fourth, and fifth characters following the function character are vernier characters for fine programming of the function within the range programmed.

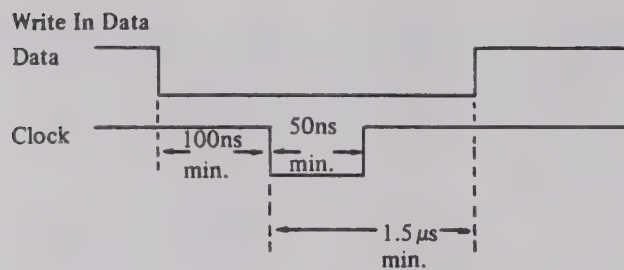
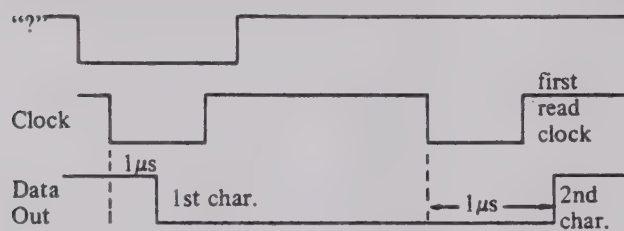
It should be noted that even though all character positions must be filled in the initial programming, when a function is edited, only those characters up to and including the character to be edited need to be programmed.

When using the Model 1501A with a paper tape reader or other data source using a "rubout" character to correct errors, the "rubout" will be ignored and not counted as a character. If using the Model 1501A in a party-line bus with other instruments such as the Model AMC 4001 Power Supply, the rubout character cannot be used in the program for these units.

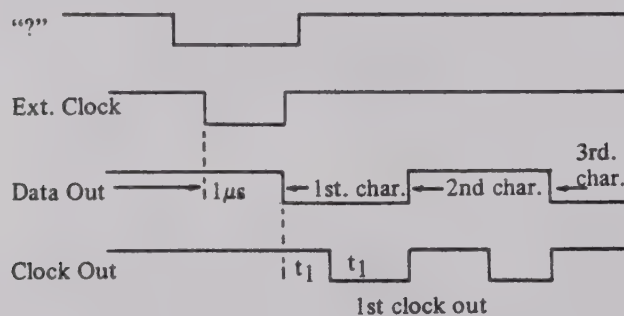
IV INPUT REQUIREMENTS

- a. Data Input. The ASCII programming option is compatible with TTL logic levels, and is normally supplied with ground true logic. High true, greater than +2.5 V, can be selected by an internal jumper. Each programming input is a standard TTL load. High level input is +5.0 V maximum.
- b. Data Output. The data output is from open collector devices capable of sinking 300 mA. True level is normally ground. Positive true is selected by an internal jumper.
- c. Strobe (Clock) Timing is shown below.

Strobe (Clock) Timing

**Read Out Data - External Clock**

The first data character is valid 1 μ s after the "?" clock is received, and remains valid until 1 μ s after the next clock pulse is received.

Read Out Data - Internal Clock

The first data character is valid 1 μ s after the external data clock. The internally-generated clock is a square wave, and the data out changes at the trailing edge of the clock pulse. The first clock out occurs at one-half the clock period. The internal clock frequency may be adjusted internally by changing the value of R26 and C4 on schematic diagram 140-22315. The maximum clock frequency is 500 kHz. The clock is normally shipped with a clock frequency of approximately 1.4 kHz (700 μ s period). In this case, the first clock occurs about 350 μ s after the "?" character is clocked in.

V VERNIER PROGRAMMING

- a. Frequency. The basic ranges change in decades, beginning with 0.5 Hz and ending with 50 MHz. Because of the "5" relationship of the ranges and the "10" relationship of the vernier programming, a calculation must be made to determine the proper three-digit vernier, multiply the required frequency by two and take the three most significant digits as the vernier program. For example, if the required frequency is 260 kHz, the required program on the 50 kHz-500 kHz is 2×260 , or 520. On the lower ranges, the frequency should be converted into Hz before multiplying (e.g., 1.87 kHz to 1870 Hz).
- b. Delay/Width. The delay and width vernier programming is straightforward, with a vernier program of 100 corresponding to the low end of the range and a program of 999 corresponding to the high end of the range. For example, a width or delay of 250 ns is programmed as 250 on the 100 ns-1 μ s range.
- c. Amplitude Programming. The basic (unattenuated) amplitude range is 5 V with 000 vernier and 9.99 V with 999 vernier. To determine the vernier for a given amplitude, including attenuation use the formula below:

$$\text{Ampl. Vernier} = \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) - 5}{.005}$$

- d. Offset Programming. The range of offset programming is from 0 to 5 V. The vernier program is the required offset value in volts, multiplied by 200. For example, if the required offset is 200 mV, the vernier is 200×0.2 , or 040.
- e. Leading and Trailing Edge Ramps. Since the leading and trailing edge ramps of the Model 1501A are constant slope with respect to changes in amplitude vernier and constant risetime with respect to changes in attenuation,

a calculation must be made to determine the program for a given combination of amplitude and rise/fall time. The fastest leading and trailing edge times are obtained at a vernier of 999, and the slowest times at a vernier of 100. To determine the proper vernier, use the following formula:

$$\text{Ramp Rate} = \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) \times K}{\text{rise or fall time}}$$

where "K" = .8 for 10-90%, K=.6 for 20-80%, etc.

Required Amplitude: 800 mV

Required 10-90% risetime: 20 ns

Step 1. Determine attenuation value by inspecting Table A4-1. An 800 mV output will be obtained on Range 4 which has an attenuation value of 8.

Step 2. Set Attenuator to Range 4.

Step 3. Determine amplitude vernier setting using the attenuation value found in Step 1.

$$\begin{aligned} \text{Ampl. Vernier} &= \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) - 5}{.005} \\ &= \frac{(.800) \times (8) - 5}{.005} \\ &= 280 \end{aligned}$$

Step 4. Set Amplitude vernier to 280.

Step 5. Determine ramp rate using:

$$\begin{aligned} \text{Ramp Rate} &= \frac{(\text{Desired Amplitude in Volts}) \times (\text{Attenuation}) \times K}{\text{risetime}} \\ &= \frac{(8.00) \times (8) \cdot 8}{20 \text{ ns}} \\ &= \frac{5.12 \text{ V}}{20 \text{ ns}} \\ &= \frac{5.12 \text{ V}}{.02 \mu\text{s}} \\ &= 256 \text{ V}/\mu\text{s} \end{aligned}$$

By inspecting Table A4-1, we find that a ramp rate of 256 V/ μ s can be obtained with Ramp Range = 1.

Step 6. Set Ramp Range to 1.

Step 7. Set Ramp vernier to 256.

NOTE: Since the vernier only varies between counts of 100 to 999, it may be necessary to multiply the Ramp Rate by either 10 or 100 to obtain the three-digit vernier setting. Example: if Ramp Rate = 24 V/ μ s, then Vernier = $24 \times 10 = 240$.

VI ASCII CIRCUIT DESCRIPTION

- a. Block Diagram Level. (See Figure A4-1) The block diagram contains the major functions performed along with the IC numbers which make up the logic. The diagram is divided by a dotted line showing which parts of the logic are located on each of the two cards. Basically, card B provides the box address and function decoding, and card A directs the data characters to their correct storage registers.

Eight Data Lines and a Clock Line are brought in to the Data Input Polarity Select logic. The input true state is selected here, so that the seven data lines to the Input Data Decode logic are always high-level true. If connected, the input character is checked for even parity, and an error signal generated when a parity error is detected. The parity error can also be connected to inhibit clocking that character in.

The Box Address Sequency Control insures that the three characters which have been selected as the box address have been sent in the proper order, before the interface will respond to a write or read instruction.

The Function Decode is armed by the valid box address and stores a function address. The output from the Function Decode is seven lines, one to each of the seven function storage registers. The alpha character "C" is also stored by the Function Decode.

Once a Function has been decoded, the next five characters must be numerics. Any other character will reset the Function Decode.

The Input/Output Character Counter counts the five characters and addresses the storage registers on the D/A cards.

The Data Input Control takes the least significant bit of the first character and temporarily stores it. When the second character is strobed in, its most significant bit is replaced with the first character's

LSB. The third, fourth and fifth characters are stored as full 4-bit characters. There are thus actually four characters clocked into the D/A storage registers.

The Data Output Control gates the MSB of the first and second characters (stored as one 4-bit character) to the LSB on the data lines to be read as the first character out. The other three bits are then gated to the output as the second character. Each of the other three BCD characters is then clocked out in sequence.

- b. Card B. (See schematic D140-22318). The input to the ASCII interface is through J1 on Card B. This connector is located in the upper right hand corner of the board. The clock line is also brought in thru this connector.

The inputs each have provision for a pull-up resistor to +5 V. These are normally only used when 1501A is the last instrument on the data bus.

IC 24, 25 and 1 gate in IC 16 are exclusive NOR gates. When their inputs are at the same logic level, their output is high, which is the true state for data at their output. The common line which is connected to one input of each of the input gates, is tied to ground for low-true logic input, or +5 V for high-true logic. This is done with a single wire as indicated by S1.

IC 22 is a 8-Bit Parity Tree. Its output, pin 8, is high as long as there is an even number of its inputs high. If the output of IC 16, pin 8, is connected to pin 4 of IC 4, via S3, then a non-even parity character inhibits the clock one-shot, IC 4, from strobing that character. For even-parity error signal, IC 16, pin 8 is connected to IC 15, pins 6 and 7, via S2. The output from IC 22, pin 6, is for odd parity checking.

The rub-out detector is IC 23. If all its inputs are high, its output, pin 8, is low and inhibits the clock one-shot, IC 4 from strobing that character.

The 3 least significant bits are decoded to 1-of-8 by IC 10. The next 2 bits, 4 and 5, are decoded to 1-of-4 by IC 17, output pins 1, 2, 3, and 4. These lines are designated A0 thru A7, and B0 thru B3. Two of these lines are connected to the box address gates of IC 11 and IC 12 via jumper wires to define the box address. The schematic shows the connections for box address PG1.

Input data bits 5, 6, and 7 are decoded by IC 21, to determine whether a character is alpha or numeric. These outputs are used as part of the box address decoding and also the function decoding.

(1) Box Address Sequence Control. Initially, the binaries of IC 18 are in a reset state. Output pin 12 of IC 17 will be low. If a "P" is decoded, pin 6, IC 12, will go high, forcing pin 8, IC 12 low. This allows the clock on pin 9, IC 19, to advance the sequence counter, IC 18. Output pin 13, IC 17 will then be low. If the next character is not a "G", then the clock on pin 4, IC 20, will reset the sequence counter. If the proper three characters are received, then pin 14, IC 17, will go low, indicating the box has been addressed and will inhibit any further clocks from resetting the sequence counter; via pin 5, IC 20.

Pin 3, IC 1, will now be low which will allow the next alpha character, decoded via IC's 1, 2, and 3, the Function decode, to be strobed into the proper flip-flop of IC 8, or 9. When a Function has been selected, the output of IC 7, pin 8, inhibits any more clocks to the Function flip-flops. If the next character is not a numeric, the Function flip-flop is reset by the output from IC 20, pin 8.

If the 5 characters following the Function alpha character are all numeric, the Function Flip-flop is reset after the fifth character by the Last Digit reset signal on pin B17 of the P.C. connector.

(2) Clock Timing. All internal clocking is derived from the clock one-shot, IC 4, pin 6. Data to the internal storage registers is strobed in on the leading, or negative-going edge of IC 4, pin 6. The box address and the Function characters are strobed at the trailing edge. The characters must therefore be valid at the time of the external clock and remain valid for the width of the one-shot. The one-shot is normally set for approximately 1 μ sec, but may be changed by changing the RC time constant circuit of R11 and C8.

c. Card A. (See schematic D1140-22315)

(1) Writing in Data. The initial state of the character counter, IC 5 and one-half of IC 4, is set when the Function Selected line on pin B18 of the P.C. connector is low. When a function has been addressed, this line goes high at the trailing edge of the clock. This enables the input decoder IC 19, via pin 7. Pin 5 of IC 19 will then go low. Pin 11, IC 19, will

Option 01 AON ASCII Programming — Model 1501A

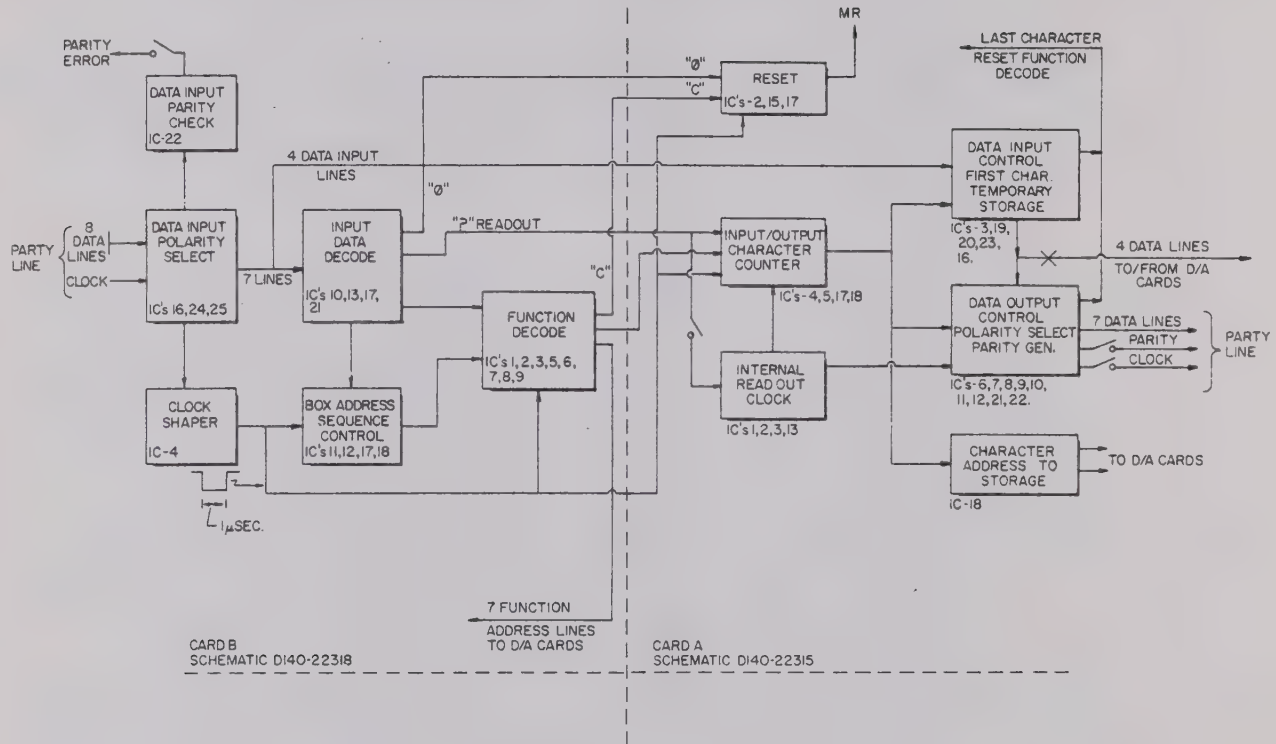


Figure A4-1

be high, forcing the clock input of IC 3, pin 3, low. This is the first character, LSB, temporary storage. At the trailing edge of the next character clock, the character counter is advanced and pin 11 of IC 19 goes low which clocks the LSB into IC 3, pin 2. Pin 11, IC 20 also goes high, enabling the input gates for the 3 least significant bits. This line also goes to Card B, via pin B14, where it enables the next four clocks to strobe data into the storage registers.

When the next clock arrives, bits 1, 2, and 3 are present at the output, pins 3, 11, and 8 of IC 23. The temporarily stored first character's LSB is present at pin 11, IC 16, as it is stored along with the other bits on the leading edge of the second character clock.

On the trailing edge of the second character clock, the character counter is again advanced and pin 12, IC 19 goes low which enables the MSB of the data via IC 23, pin 4, and also holds the output of IC 20, pin 11 high.

At the trailing edge of the fifth data clock, the character counter is advanced and IC 19, pin 3 goes low, resetting the Function Decode Flip-flop. The Function Selected line goes low, re-initializing the character counter and disabling the input decode control, IC 19. The output from IC 19, pin 7, is therefore a negative-going spike generated at the trailing edge of the character clock.

(2) Reading Out Data. Read out is initiated by a "?" immediately following a Function character. The Read Out signal on pin A2 will be high, inhibiting the Character Clock from advancing the character counter, via IC 17, pin 1. IC 19, pin 5, will be low, thus clocking the high level on IC 4, pin 2, into the Flip-flop. IC 4, pin 5 goes high, enabling the Data Output decode Control, IC 6. IC 4, pin 6 goes low, disabling the Data Input decode control IC 19. The first 4 bits of data from the selected function are then present at pins BK, BJ, BH and BL. The 3 LS bits are inhibited by the high output from IC 7, pin 11. The MSB on IC 8, pin 2, is gated to the output LSB. When the first of the five data clocks arrives, the data output will either be a 1 or a 0, depending on the Mode bit that is in storage.

The character counter is advanced and IC 6, pin 11 goes low, enabling the 3 least significant bits and inhibiting the MSB. The next data clock strobes only the 3 least significant bits. At its trailing

edge, the character counter is advanced and IC 6, pin 12, goes low. This enables the MSB to be present on the data bus. The character counter is decoded by IC 18, pins 8 and 11 to address the next three characters from storage.

At the trailing edge of the fifth readout clock, IC 6, pin 3 goes low, resetting the Function Decode Flip-flop, ending the readout sequence.

During a readout sequence, data bus lines 5 and 6 are forced to be only '1's, and bit 7 is forced to be a '0' bit.

(3) Readout With Internal Clock. The internal clock is generated by turning on the multivibrator, IC 1, and dividing it down with Flip-flop IC 3. IC 13, pin 1 is strapped to +5 V, at S3. IC 18, pin 1 is connected to IC 3, pin 9, which then is the clock used to step the character counter. The clock multivibrator is turned on when readout signal on IC 4, pin 2 is clocked in.

(4) Master Reset. When power is applied, Master Reset is held low by capacitor C 6 being charged by the input current of IC 20, pin 4. The output from pins 6 and 8 of IC 16 reset the box address sequence counter and the Function Decode Flip-flop.

(5) "CO" Reset. "C" is decoded and stored as all other box functions. At the next character clock, a Master Reset will be generated via IC 15, pin 11, if the character is a zero. At the trailing edge of the clock, the output from IC 13, pin 11, will be a negative pulse determined by R6 and C5, which will reset the Function Decode Flip-flops.

Table A4-1 ASCII Programming Format

Function	ID Character	Mode Control	Range Character	Range	Vernier Character
Frequency	F	0=Internal Clock 1=External Clock	0	0.5-4.995 Hz	100-999
			1	5-49.95 Hz	100-999
			2	50-499.5 Hz	100-999
			3	0.5-4.995 KHz	100-999
			4	5-49.95 KHz	100-999
			5	50-499.5 KHz	100-999
			6	0.5-4.995 MHz	100-999
			7	5-49.95 MHz	100-999
Delay	D	0=Single Pulse 1=Double Pulse	0	10-99.9 ns	100-999
			1	100-999 ns	100-999
			2	1-9.99 μ s	100-999
			3	10-99.9 μ s	100-999
			4	100-999 μ s	100-999
			5	1-9.99 ms	100-999
			6	10-99.9 ms	100-999
			7	100-999 ms	100-999
Width	W	0=Inverted Pulse 1=Normal Pulse	0	10-99.9 ns	100-999
			1	100-999 ns	100-999
			2	1-9.99 μ s	100-999
			3	10-99.9 μ s	100-999
			4	100-999 μ s	100-999
			5	1-9.99 ms	100-999
			6	10-99.9 ms	100-999
			7	100-999 ms	100-999
Unattenuated Ramp Slope:					
Leading Edge (Neg Ramp)	L	0=Gate Off 1=Gate On	0	Uncalibrated Range*	100-999
			1	0.1-0.999 V/ns	100-999
			2	10.0-99.9 V/ μ s	100-999
			3	1.0-9.99 V/ μ s	100-999
			4	0.1-0.999 V/ μ s	100-999
			5	10.0-99.9 V/ms	100-999
Trailing Edge (Pos Ramp)	T	N/A	N/A		
Attenuation and Amplitude	A	0=Negative Pulse 1=Positive Pulse	0	(x128) 40-80 mV	000-999
			1	(x64) 80-160 mV	000-999
			2	(x32) 156-312 mV	000-999
			3	(x16) 312-625 mV	000-999
			4	(x8) 0.62-1.25 V	000-999
			5	(x4) 1.25-2.5 V	000-999
			6	(x2) 2.5-5.0 V	000-999
			7	(x1) 5.0-10.0 V	000-999
Offset	O	N/A	0	No Offset	000-999
			2	0 to +5 V	000-999
			4	0 to -5 V	000-999

CO-Reset

Period "." resets instrument address

"?" following a function character initiates readout of data

"rubout" character is ignored in Model 1501A

Note

References to Neg Ramp and Pos Ramp refer to leading and trailing edges, respectively, in positive and negative normal modes. In positive and negative inverted modes, the negative ramp becomes the trailing edge and the positive ramp becomes the leading edge.

*The uncalibrated range gives minimum risetime (approx 3 ns) when 999 vernier is programmed. Intermediate values give risetimes from 3 ns and 30 ns, but programming is non-linear.

Table A4-2 Program Input Connection

J110 and J111 on the rear panel can be used interchangeably as input or output connectors.

Pin No.	Connection
1	ASCII Bit 1 Input/Output
2	Gnd
3	ASCII Bit 2 Input/Output
4	Gnd
5	ASCII Bit 3 Input/Output
6	Gnd
7	ASCII Bit 4 Input/Output
8	Gnd
9	ASCII Bit 5 Input/Output
10	Gnd
11	ASCII Bit 6 Input/Output
12	Gnd
13	Not used in Model 1501A
14	ASCII Bit 7 Input/Output
15	Gnd
16	ASCII Bit 8 Output (Parity Check)
17	Gnd
18	Clock Input
19	Gnd
20	Not used in Model 1501A
21	Gnd
22	Not used in Model 1501A
23	Not used in Model 1501A
24	Not used in Model 1501A
25	Gnd

Note:
Rear-panel connectors mate with Cinch DBM-25P.

JOB NO.	ASSEMBLIES REQ'D	COST CENTER	DATE

WHERE USED
1501A
1504

INDEX ☒

ASSEMBLY ☐

SPEC. ASSEM. ☐

B/M PAGE _____

COPY DATE 3-28-78

ASSEMBLY NO. 350-21920

E.C.O. 78-041

DESCRIPTION MOD KIT, ASCII BCD GND TRUE/POS TRUE

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A		ADD to INDEX							
B	*401-22314	ASCII 'A' Board Assy	A308	1					
C	*401-22317	ASCII 'B' Board Assy	A309	1					
D	*401-22619	Serial D/A Board Assy	A305-307, A311-314	7					
E									
F		ADD to Rear Panel Assy							
G	*249-21386	Rear Subpanel Assy		1					
H									
I		ADD to Standard Accessories							
J	146-26302	Documentation List	Prod Ref						
K	700-00304	Connector, 25 Pin M Cinch	P110,111	2					
L	700-00338	Slidelock, Conn	(P110,111)	2					
M	891-00309	Cover, Conn	(P110,111)	2					
N									
O									
P									
Q									
R									
S									
T									

NOTE: MARKETING OPTION 01-AØN/AØP
*SEE 1500 Series

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

WHERE USED
1500 Series

INDEX ☐ ASSEMBLY ☒ SPEC. ASSEM. ☐
 ASSEMBLY NO. 249-21386
 DESCRIPTION ASSEMBLY SUB-PANEL REAR

B/M PAGE
 COPY DATE 4-17-73
 E.C.O. 76-050

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	248-21382	Panel		1					
B	144-21384	Silkscreen	Prod Ref						
C									
D	700-00337	Post, Slide Lock		2					
E	706-21378	Cable Assy, Dual 34 Pin	J110,J111	1					
F									
G	140-22748	Schematic	Prod Ref						
H									
I									
J									
K									
L									
M									
N									
O									
P									
Q									
R									
S									
T									

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

WHERE USED
1500 Series

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ASSEMBLY ☒

SPEC. ASSEM. ☐

B/M PAGE _____

COPY DATE 4-30-73

E.C.O.

ASSEMBLY NO. 401-22314

DESCRIPTION INTERFACE A ASCII BOARD ASSEMBLY

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	400-22313	PC Board		1					
B	401-22314	Assembly Drawing	Prod Ref						
C	140-22315	Schematic	Prod Ref						
D									
E	311-00009	Cap, Cerm 500pf	C5,11	2					
F	311-00021	Cap, Cerm .05 μ f 75V	C4	1					
G	311-00041	Cap, Cerm .1 μ f/12V	C2,3,7-9	5					
H	318-00005	Cap, Tant 10 μ f 20V	C6	1					
I	318-00004	Cap, Tant 27 μ f 10V	C1	1					
J	335-00022	Choke, 1 μ h	L1	1					
K	376-00022	Diode, 1N914B	CR1	1					
L									
M	595-00101	Resistor 100 Ω $\frac{1}{2}$ W 5%	R6,27	2					
N	595-00104	Resistor 100K $\frac{1}{2}$ W 5%	R14	1					
O	595-00122	Resistor 1.2K $\frac{1}{2}$ W 5%	R7-10 18-23	10					
P	595-00222	Resistor 2.2K $\frac{1}{2}$ W 5%	R11-13, 25 15-17,24,	8					
Q	595-00303	Resistor 30K $\frac{1}{2}$ W 5%	R26	1					
R	595-00511	Resistor 510 Ω $\frac{1}{2}$ W 5%	R3	1					
S									
T									

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

WHERE USED
1500 Series

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ASSEMBLY NO. 401-22314

DESCRIPTION INTERFACE A ASCII BOARD ASSEMBLY

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FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTEN-SION	SHORT
A	665-00053	IC MC 3000P	IC 2,7,20	3					
B	665-00056	IC MC 3060P	IC3-5	3					
C	665-00078	IC MC 3004P	IC13,16,18,23	4					
D	665-00084	IC MC 3022P	IC9,10,24	3					
E	665-00100	IC SN75453P	IC8,11,12,14,21,22	6					
F	665-00110	IC MC 3002P	IC15,17	2					
G	665-00130	IC MC 8601P	IC1	1					
H	665-00123	IC MC 4038P	IC6,19	2					
I									
J	450-00308	Jack, Brown	TP5	1					
K	450-00309	Jack, Red	TP4	1					
L	450-00310	Jack, Orange	TP2	1					
M	450-00317	Jack, Black	TP1, TP3	2					
N									
O									
P									
Q									
R									
S									
T									

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

WHERE USED
1500 Series

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ASSEMBLY ☒

SPEC. ASSEM. ☐

ASSEMBLY NO. 401-22317

DESCRIPTION INTERFACE B ASCII BOARD ASSEMBLY

B/M PAGE
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E.C.O. 76-050
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FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	400-22316	PC Board		1					
B	401-22317	Assembly Drawing	Prod Ref						
C	140-22318	Schematic	Prod Ref						
D									
E	311-00008	Cap, Cerm 150pf	C9	1					
F	311-00074	Cap, Cerm .01μf 100V	C2-7	6					
G	318-00005	Cap, Tant 10μf 20V	C1	1					
H	335-00022	Choke 1μh	L1	1					
I	595-00102	Resistor 1K ½W 5%	R1-9	9					
J	595-00183	Resistor 18K ½W 5%	R11	1					
K	595-00222	Resistor 2.2K ½W 5%	R10,12-20	10					
L	665-00140	IC SN7427N	IC1-3 13,14	5					
M	665-00130	IC MC8601P	IC4	1					
N	665-00078	IC MC 3004P	IC5,6	2					
O	665-00090	IC SN7430N	IC7,23	2					
P	665-00144	IC MC4015P	IC8,9	2					
Q	665-00057	IC MC 4006P	IC10	1					
R	665-00148	IC SN7425N	IC11,12	2					
S	665-00100	IC SN75453P	IC15	1					
T	665-00084	IC MC3022P	IC16,24,25	3					

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

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ASSEMBLY NO. 401-22317

DESCRIPTION INTERFACE B ASCII BOARD ASSEMBLY

B/M PAGE

COPY DATE 4-30-73

E.C.O. 78-048

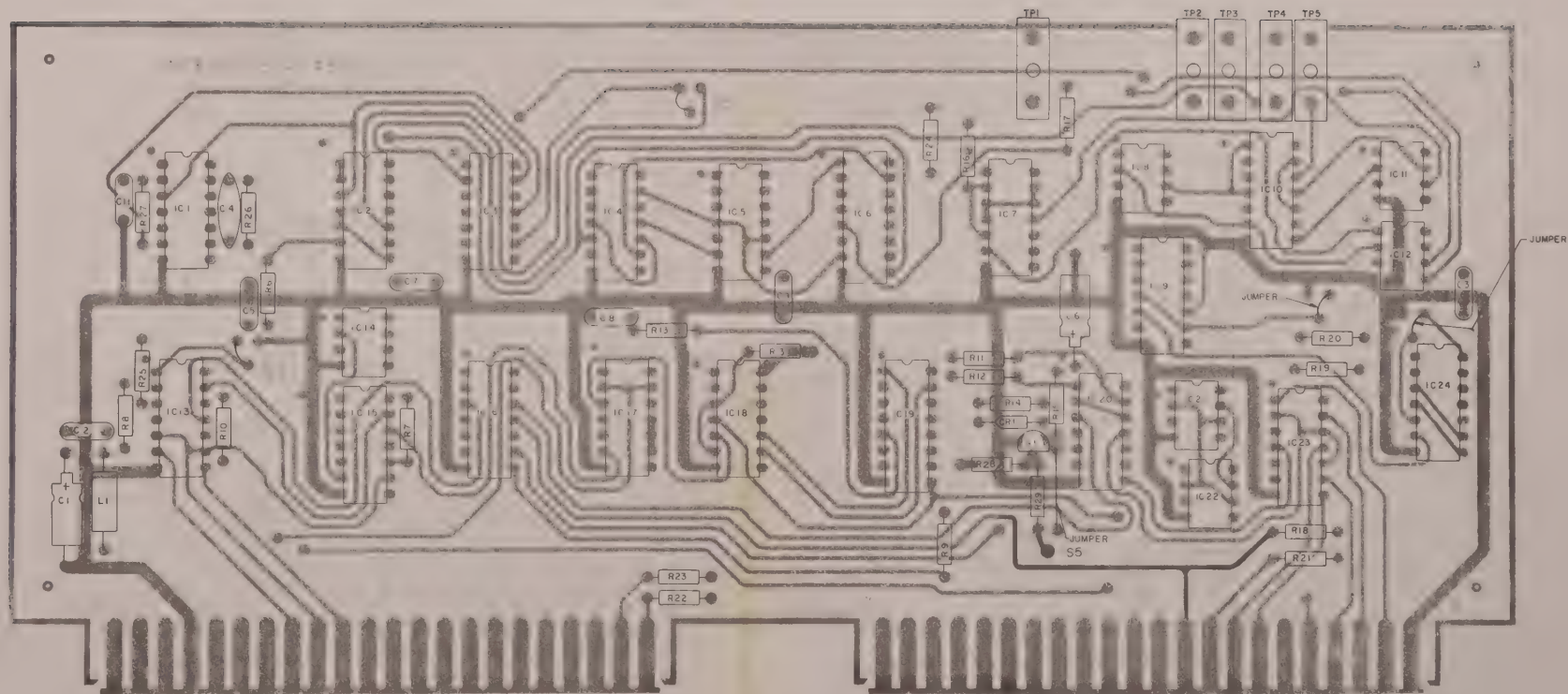
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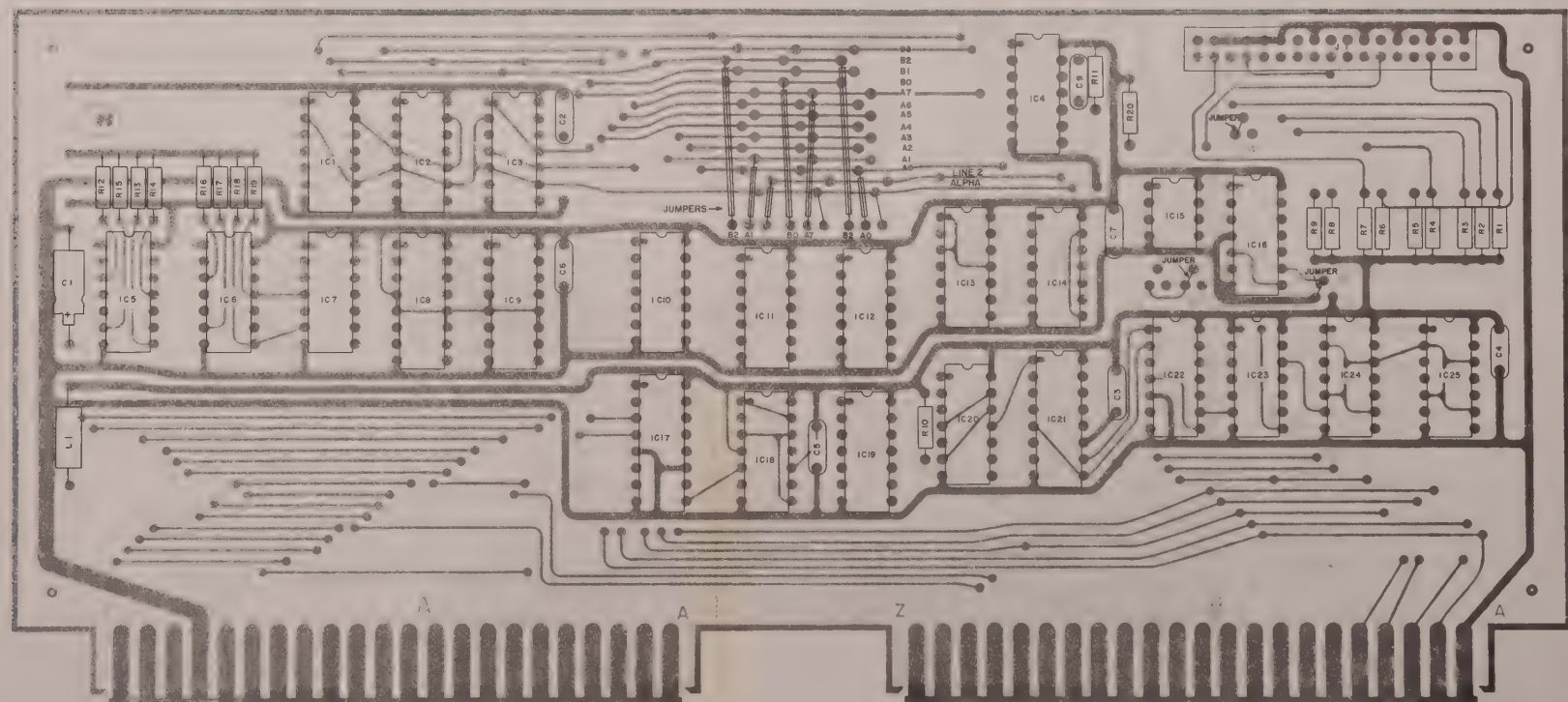
DATE

RELEASED TO

DATE

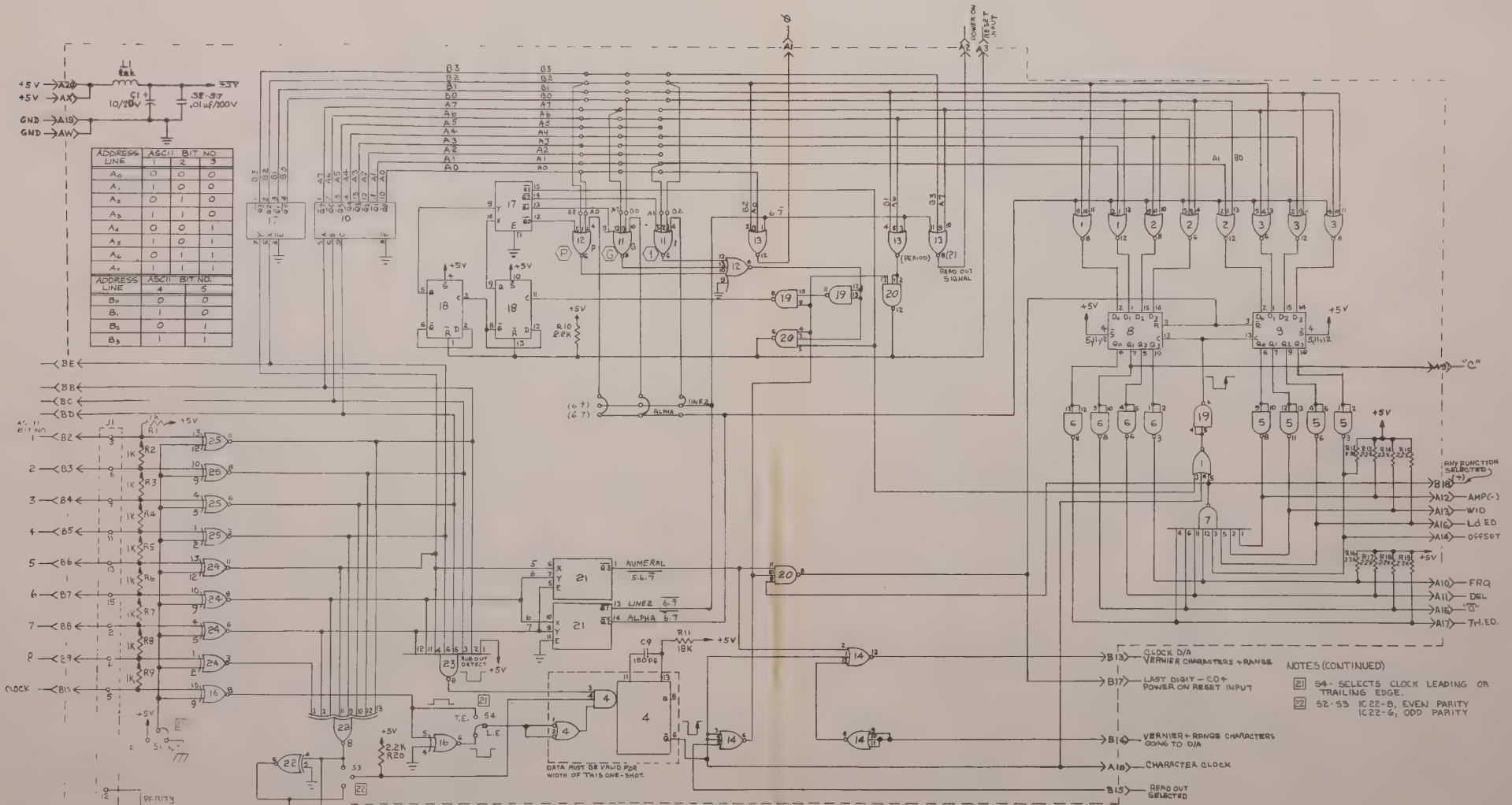
ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	665-00053	IC MC3000P	IC19	1					
B	665- 00114	IC MC3007P	IC20	1					
C	665-00150	IC MC4008P	IC22	1					
D	665-00149	IC MC4007P	IC17,21	2					
E	665-00056	IC MC3060P	IC18	1					
F									
G	700-00 262	Connector, 34 Pin Berg	J1	1					
H									
I									
J									
K									
L									
M									
N									
O									
P									
Q									
R									
S									
T									





ASSEMBLY DRAWING
INTERFACE 8 (ASCII)

1501A
D-401-
22317 C



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTANCES IN OHMS, 1/4 W, 5 %
2. ALL CAPACITORS IN μ F
3. IC 1, 2, 3, 13, 14 ARE SN7425N
4. IC 14 IS MC801P
5. IC 5, 6, ARE MC3004P
6. IC 7, 23 ARE MC7430
7. IC 8, 9 ARE MC4015P
8. IC 10 IS MC4006P
9. IC 11, 12 ARE SN7425N

10. IC 15 IS SN75453P +5V PIN 8, GND PIN 4
11. IC 16, 24, 25 ARE MC3022P
12. IC 19, IS MC3000P
13. ALL +5V PIN 14, ALL GND PIN 7, EXCEPT*
14. IC 18 IS MC3060P
15. IC 20 IS MC3007P
16. IC 22 IS MC4000BP

17. IC 21, 17 ARE MC4007P +5V PIN 16 GND PIN 8

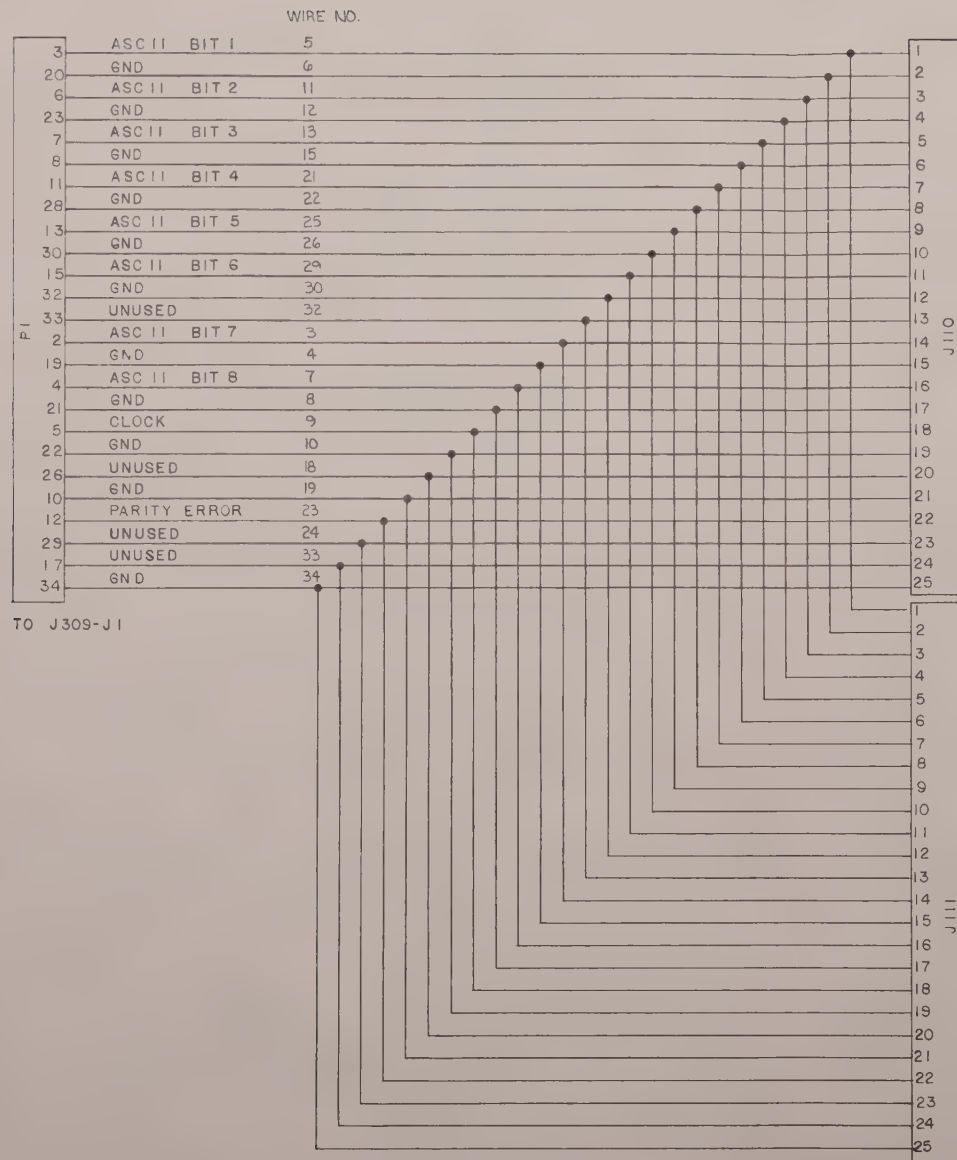
18. REF. DWGS
R.C.B. FAB. 400-22316
ASSY 401-22317

19. ADDRESS DECODE SHOWN AS "P", "G", "I".

20. BCD GND TRUE LOGIC SHOWN FOR POSITIVE TRUE LOGIC: MOVE JUMPER S1 TO +5V

NOTES (CONTINUED)

21. S4 - SELECTS CLOCK LEADING OR TRAILING EDGE.
22. S2-S3 IC22-B, EVEN PARITY IC22-G, ODD PARITY



SCHEMATIC ASC II
SUB-PANEL REAR

1501 A
140-
C-22748 B

APPENDIX A-5
SERIAL DIGITAL TO ANALOG CONVERTER

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

WHERE USED
1500 Series

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SPEC. ASSEM. ☐

ASSEMBLY NO. 401-22619

DESCRIPTION SERIAL D/A CONVERTER BCD ASSEMBLY

B/M PAGE
COPY DATE 5-31-73
E.C.O. 74-011
76-050
77-012
78-061

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	400-22618	PC Board		1					
B	401-22619	Assembly Drawing	Prod Ref						
C	140-22620	Schematic	Prod Ref						
D									
E	311-00001	Cap, Cerm 10pf 1KV	C3	1					
F	311-00074	Cap, Cerm .01μf 100V	C2,5,6, 8,9	5					
G	318-00004	Cap, Tant 27μf 10V	C1	1					
H	318-00005	Cap, Tant 10μf 20V	C4,7	2					
I	335-00022	Choke 1.0μh	L1	1					
J	495-00054	Socket, IC 16 Pin	J1	1					
K									
L	551-00035	Potentiometer 500Ω 89PR	R30	1					
M	551-00040	Potentiometer 1K 89PR	R27	1					
N	595-00100	Resistor 10Ω ½W 5%	R28,33	2					
O	595-00153	Resistor 15K ½W 5%	R32	1					
P	595-00165	Resistor 1.6M ½W 5%	R11	1					
Q	595-00222	Resistor 2.2K ½W 5%	R13-24	12					
R	595-00335	Resistor 3.3M ½W 5%	R12	1					
S	595-00394	Resistor 390K ½W 5%	R9	1					
T	595-00512	Resistor 5.1K ½W 5%	R34, 35	2					

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

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78-006

78-058

ASSEMBLY NO. 401-22619

DESCRIPTION SERIAL D/A CONVERTER BCD ASSEMBLY

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	595-00824	Resistor 820K $\frac{1}{4}$ W 5%	R10	1					
B									
C	611-00001	Resistor 4K .05%	R1	1					
D	611-00002	Resistor 8K .1%	R2	1					
E	611-00003	Resistor 16K .1%	R3	1					
F	611-00004	Resistor 32K .1%	R4	1					
G	586-01653	Resistor 165K 1/8W 1% MF	R7	1					
H	586-03163	Resistor 316K 1/8W 1% MF	R8	1					
I	586-03321	Resistor 3.32K 1/8W 1% MF	R25	1					
J	586-04221	Resistor 4.22K 1/8W 1% MF	R31	1					
K	586-06191	Resistor 6.19K 1/8W 1% MF	R26	1					
L	586-09091	Resistor 9.09K 1/8W 1% MF	R29	1					
M	586-04022	Resistor 40.2K 1/8W 1% MF	R5	1					
N	586-08062	Resistor 80.6K 1/8W 1% MF	R6	1					
O									
P	663-00070	Transistor 2N3904	Q1-12	12					
Q									
R	665-00172	IC 74H01	IC 5	1					
S	665-00079	IC N5741CT	IC 8	1					
T	665-00050	IC 7402	IC 12	1					

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75-227

77-012

78-061

ASSEMBLY NO. 401-22619

DESCRIPTION SERIAL D/A CONVERTER BCD ASSEMBLY

FILLED BY DATE RELEASED TO DATE

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	665-00334	IC SN74LS04N	IC 13, 15	2					
B	665- 00341	IC SN74LS175N	IC9-11,14	4					
C	665-00369	IC SN74LS138N	IC 4	1					
D	665-00339	IC SN74LS153N	IC 6,7	2					
E	665-00152	IC N8266B or MC7266P	IC 16	1					
F	665-00153	IC N74157B or MC74157P	IC 1-3	3					
G									
H	495-00027	Amp Pins	XIC8	8					
I	496-00043	Transistor Pad	XIC8	1					
J									
K									
L									
M									
N									
O									
P									
Q									
R									
S									
T									

APPENDIX A-6

PARALLEL DIGITAL TO ANALOG CONVERTER

I PARALLEL D/A CONVERTER

The operation of the D/A converter is conventional. A negative true input is applied to ICs 1 through 3. The output of these ICs control the transistor switches, Q2 through Q13, which directly program the weighted resistor network, R4 through R15, provides a 1248 BCD coded input to the summing junction for operational amplifier IC 1. If a 000 count is programmed, none of the transistors are turned on and there is no current flowing through any of the resistors. As a result, the current through resistors R40 and R41 is balanced against the current flowing in R45. The current in R45 is proportional to the voltage difference between the output of the operational amplifier and the inverting input. The voltage of the inverting input will be exactly the same as the voltage of the non-inverting input when the system reached equilibrium. Thus, if a proper current is supplied via R40, the output voltage of the operational amplifier will have to be exactly 0 volts when none of the resistors in the weighted ladder network are activated. When a resistor is connected to ground via the switching transistor, it reduces the total amount of current flowing towards the negative input of the operational amplifier and hence causes less current to flow through R45. This means the output voltage of IC 1 must raise to exactly compensate for the resistor which has been connected to ground. The output voltage from the card is directly proportional to the digital input control. Range line buffering is provided by IC' 5-8.

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ASSEMBLY NO. 401-21212

E.C.O. 76-050

77-005

77-048

DESCRIPTION PARALLEL D/A CONVERTER BOARD BCD
ASSEMBLY

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHOR
A	400-21209	PC Board		1					
B	401-21212	Assembly Drawing	Prod Ref						
C	140-21213	Schematic	Prod Ref						
D									
E	311-00001	Cap, Cerm 10pf 10V	C6	1					
F	311-00074	Cap, Cerm .01μf/100V	C1,3,5	3					
G	318-00005	Cap, Tant, 10μf 20V	C2,4	2					
H									
I	495-00059	IC Socket, 16 Pin	J1	1					
J	496-00043	Transistor Pad	XIC1	1					
K	551-00035	Beckman 79PR Potentiometer 500Ω	R43	1					
L	551-00040	Beckman 79PR Potentiometer 1K,	R40	1					
M	595-00100	Resistor 10Ω ½W 5%	R47,48	2					
N	595-00202	Resistor 2K ½W 5%	R2	1					
O	595-00165	Resistor 1.6M ½W 5%	R5	1					
P	595-00222	Resistor 2.2K ½W 5%	R3,16-39	25					
Q	595-00335	Resistor 3.3M ½W 5%	R4	1					
R	595-00394	Resistor 390K ½W 5%	R7	1					
S	595-00511	Resistor 510Ω ½W 5%	R1	1					
T	595-00682	Resistor 6.8K ½W 5%	R46	1					

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77-048

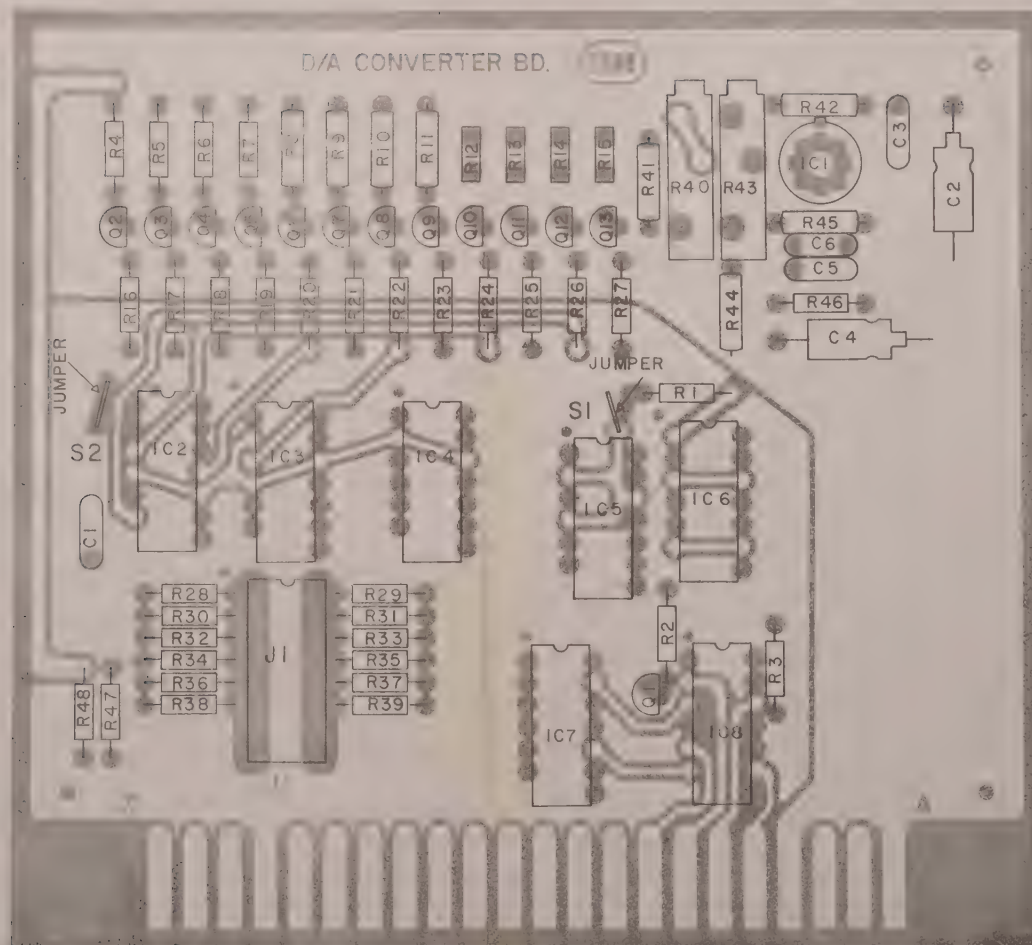
78-013

ASSEMBLY NO. 401-21212

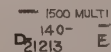
DESCRIPTION PARALLEL D/A CONVERTER BOARD BCD
ASSEMBLY

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	595-00824	Resistor 820K $\frac{1}{2}$ W 5%	R6	1					
B	611-00001	Resistor 4K .05% Vishay V53-1	R15	1					
C	611-00002	Resistor 8K .1% Vishay V53-1	R14	1					
D	611-00003	Resistor 16K .1% Vishay V53-1	R13	1					
E	611-00004	Resistor 32K .1% Vishay V53-1	R12	1					
F	586-01653	Resistor 165K 1/8W 1% MF	R9	1					
G	586-03163	Resistor 316K 1/8W 1% MF	R8	1					
H	586-03321	Resistor 3.32K 1/8W 1% MF	R45	1					
I	586-06191	Resistor 6.19K 1/8W 1% MF	R41	1					
J	586-09091	Resistor 9.09K 1/8W 1% MF	R42	1					
K	586-04022	Resistor 40.2K 1/8W 1% MF	R11	1					
L	586-08062	Resistor 80.6K 1/8W 1% MF	R10	1					
M	586-04421	Resistor 4.42K 1/8W 1% MF	R44	1					
N	663-00070	Transistor 2N3904	Q1-13	13					
O									
P	665-00383	IC 74LS86	IC 6-8	3					
Q	665-00079	IC N5741	IC 1	1					
R	665-00137	IC 74LS00	IC 2-5	4					
S									
T									



ASSEMBLY DRAWING,
PARALLEL D/A CONVERTER BD
1500 SERIES





1500 MULTI
140-
D-29877 B

APPENDIX B

OPTION 02 FRONT - PANEL CONTROLS

B-1 FREQUENCY

This set of switches controls the pulse repetition frequency from 005.0 Hz to 49.95 MHz. The fourth digit is either 0 or 5, giving half steps between the steps of the third digit. The decimal point is positioned automatically, determined by the setting of the range switch (the right-most thumbwheel switch in the group). The range switch reads directly in Hz, kHz, or MHz.

B-2 WIDTH

These switches control the pulse width, with settings of 010 ns to 9.99 ms allowable. The range switch reading directly in ns, μ s, or ms.

B-3 DELAY

The delay switches function in the same way as the WIDTH switches, controlling the time between the trigger output and the main pulse output in SINGLE pulse mode, or the spacing between the first and second pulses in DOUBLE pulse mode.

B-4 RAMPS

This set of switches consists of a common range switch with settings of x3 V/ns, V/ns, V/ μ s or V/ms and separate LEADING EDGE and TRAILING EDGE three-digit switch sections. These switches control the rate or rise and fall - not the rise or fall times. The pulse amplitude must be taken into consideration to determine settings of a given rise or fall time.

B-5 AMPLITUDE

The AMPLITUDE switches are divided into three sections; 1) POLARITY, 2) RANGE, and 3) % OF RANGE. The POLARITY section consists of two switches. The first switch selects N (normal) or I (inverted); the second switch selects +(positive-going) or - (negative-going). The RANGE switch is effectively the attenuation control. The switch selects full-scale (i.e., at maximum amplitude) ranges of 10.0V, 5.00 V, 2.50 V, 1.25 V, .625 V, .312 V, .156 V, and .078 V. The % OF RANGE switches select the amplitude within the selected range from 50.00% to 99.95%.

B-6 OFFSET

The OFFSET group of switches set the baseline offset with respect to ground. The first switch selects NEG (negative with respect to ground); POS (positive with respect to ground) and OFF (baseline at ground level). The second group of switches select the offset value from 0.000 V to 4.995 V. The fourth digit is either 0 or 5. It should be noted that the fourth digit in the FREQUENCY, AMPLITUDE, and OFFSET controls are provided for high resolution only; the basic accuracy and repeatability of the Model 1501A are unchanged.

B-7 PROGRAM MODE

The three PROGRAM MODE toggle switches allow local or remote (program) control of portions of the Model 1501A circuitry independently. This allows manual control of certain parameters while maintaining the others under external control. The three parameters which can be selected for local or remote control are: CLOCK (pulse repetition frequency); D/W (delay and width) and OUTPUT (leading/trailing edge slope, polarity, normal/inverted, attenuation, amplitude and offset).

B-8 CLOCK, GATE AND PULSE MODE

These three toggle switches select internal or external clock, gated output either on or off by external signal, and single or double pulse. It should be noted that the internal/external clock switch, the gating mode switch, and the single/double pulse switch are enabled only when the appropriate local/remote switch is in the local position. For external/ internal clock selection, the CLOCK switch must be in the local position. For gating and single/double pulse selection, the D/W switch must be in the local position.

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1501A

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ASSEMBLY NO. 350-21900

COPY DATE 3-28-78

E.C.O. 78-041

DESCRIPTION MOD KIT/SERIAL FRONT PANEL CONTROL

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	1501A	Bill of Material		1					
B									
C		ADD to INDEX							
D	**251-21049	Front Panel Assembly		1					
E									
F		ADD to Standard Accessories							
G	146-26300	Documentation List	Prod Ref						
H									
I									
J									
K									
L									
M									
N									
O									
P									
Q									
R									
S									
T									

NOTE: MARKETING OPTION-02
**SEE 1500 Series

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ASSEMBLY NO. 251-21049

COPY DATE 12-10-76

E.C.O. 77-005 77-012

DESCRIPTION DIGISWITCH FRONT PANEL CONTROL ASSEMBLY

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	250-29851	Front Panel		1					
B									
C	**249-21206	Sub Panel Assy, Front		1					
D									
E	**402-22061	Front Panel Interface Bd		1					
F									
G	630-00022	Switch, Power	S201	1					
H	630-00012	Switch, Toggle Mini	S202-207	6					
I									
J	702-29848	Wire List, Front Panel	Prod Ref						
K									
L									
M		-HARDWARE-							
N	203-00005	Screw 6-32x $\frac{1}{2}$ BHMS (5)	Prod Ref						
O	203-00037	Screw 6-32x3/8 OvHd 82°(6)	Prod Ref						
P									
Q									
R									
S									
T									

JOB NO.	ASSEMBLIES REQ'D	COST CENTER	DATE

WHERE USED
1500 Series

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ASSEMBLY NO. 249-21206

COPY DATE 12-10-76

E.C.O. 77-005

DESCRIPTION SUB PANEL ASSEMBLY, FRONT

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	248-29845	Sub Panel, Front		1					
B									
C	**640-29854	Switch Assy, Frequency	S208	1					
D	**640-29856	Switch Assy, Delay	S209	1					
E	**640-29936	Switch Assy, Ramps	S211	1					
F	**640-29942	Switch Assy, Amplitude	S212	1					
G	**640-29939	Switch Assy, Offset	S213	1					
H	**640-29952	Switch Assy, Width	S210	1					
I									
J									
K		-HARDWARE-							
L	203-00006	Screw 6-32x $\frac{1}{2}$ FHMS (5)	Prod Ref						
M	475-00054	Standoff (5)	Prod Ref						
N									
O									
P									
Q									
R									
S									
T									

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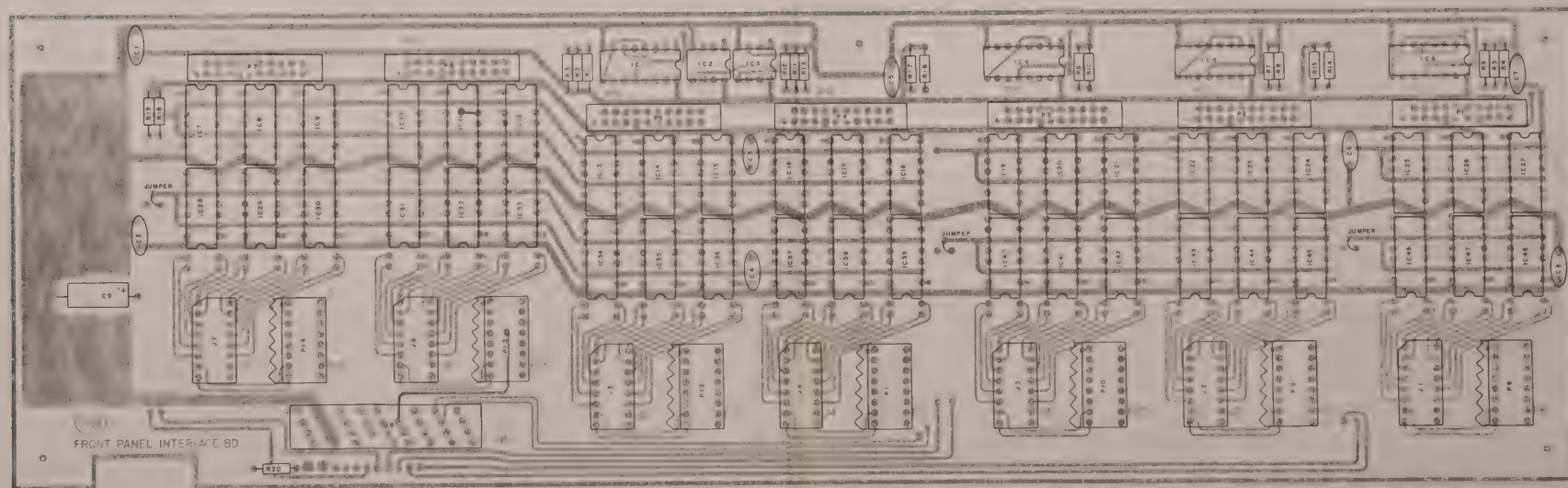
E.C.O. 77-005

ASSEMBLY NO. 402-22061

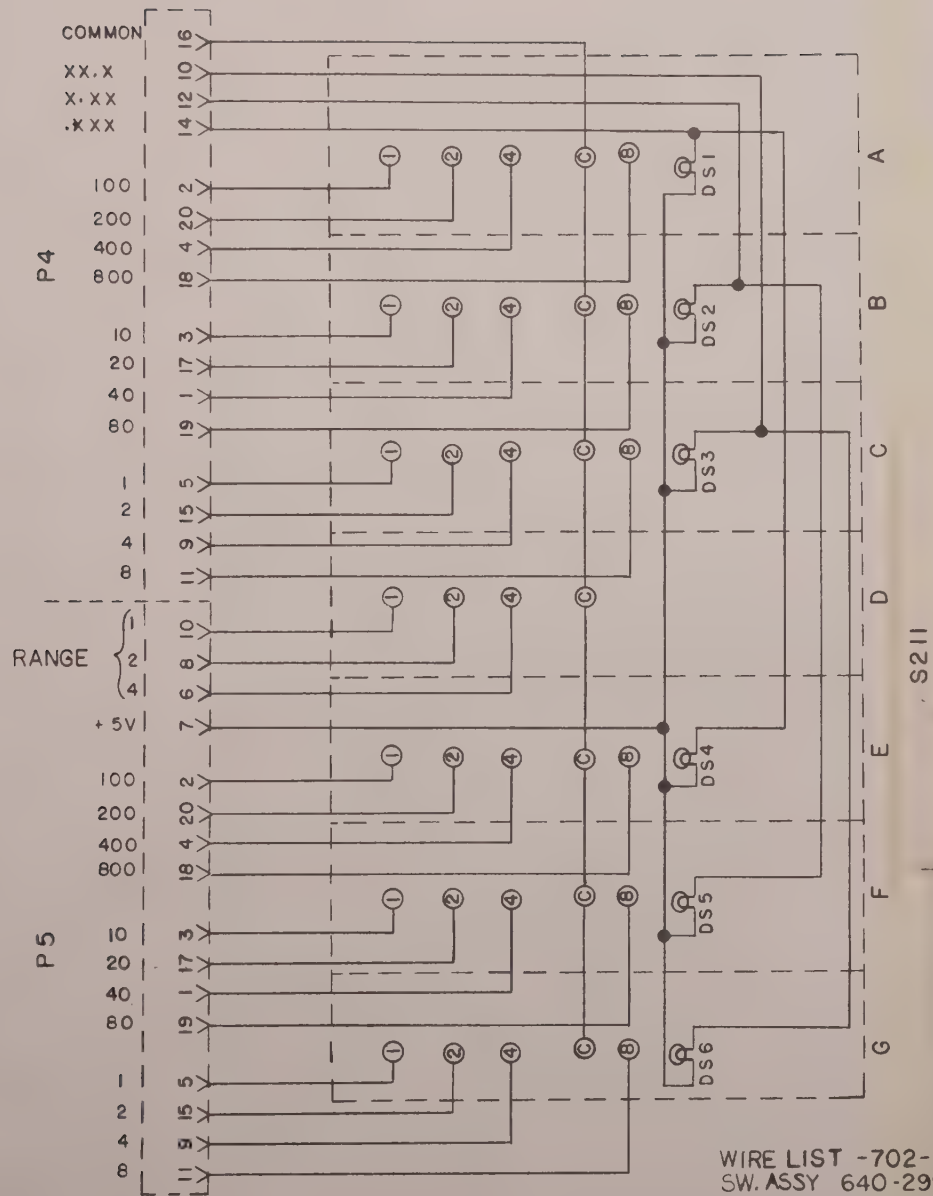
DESCRIPTION FRONT PANEL INTERFACE BOARD ASSEMBLY

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	400-22060	PC Board		1					
B	402-22061	Assembly Drawing	Prod Ref						
C	140-22062	Schematic	Prod Ref						
D									
E	311-00074	Cap, Cerm .01 μ f	C1-8	8					
F	318-00005	Cap, Tant 10 μ f 20V	C9	1					
G	495-00054	Socket, IC 16 Pin	J1-7	7					
H	595-00047	Resistor 4.7 Ω $\frac{1}{4}$ W 5%	R20	1					
I	595-00222	Resistor 2.2K $\frac{1}{4}$ W 5%	R1-3	3					
J	595-00471	Resistor 470 Ω $\frac{1}{4}$ W 5%	R14-19	6					
K	595-00511	Resistor 510 Ω $\frac{1}{4}$ W 5%	R4-13	10					
L	665-00037	IC MC 849P	IC7-48	42					
M	665-00080	IC SN74145N	IC1,4-6	4					
N	665-00100	IC SN75453N	IC 2,3	2					
O	700-00127	Connector Transition 20 Pin Header 3M3428-2002	P1-7	7					
P									
Q	706-21207	1/1 16 Pin Cable Assy Flat Ribbon	(P8-14)	1					
R	706-21208	34 Pin Cable Assy Flat Ribbon	(J8)	1					
S									
T									



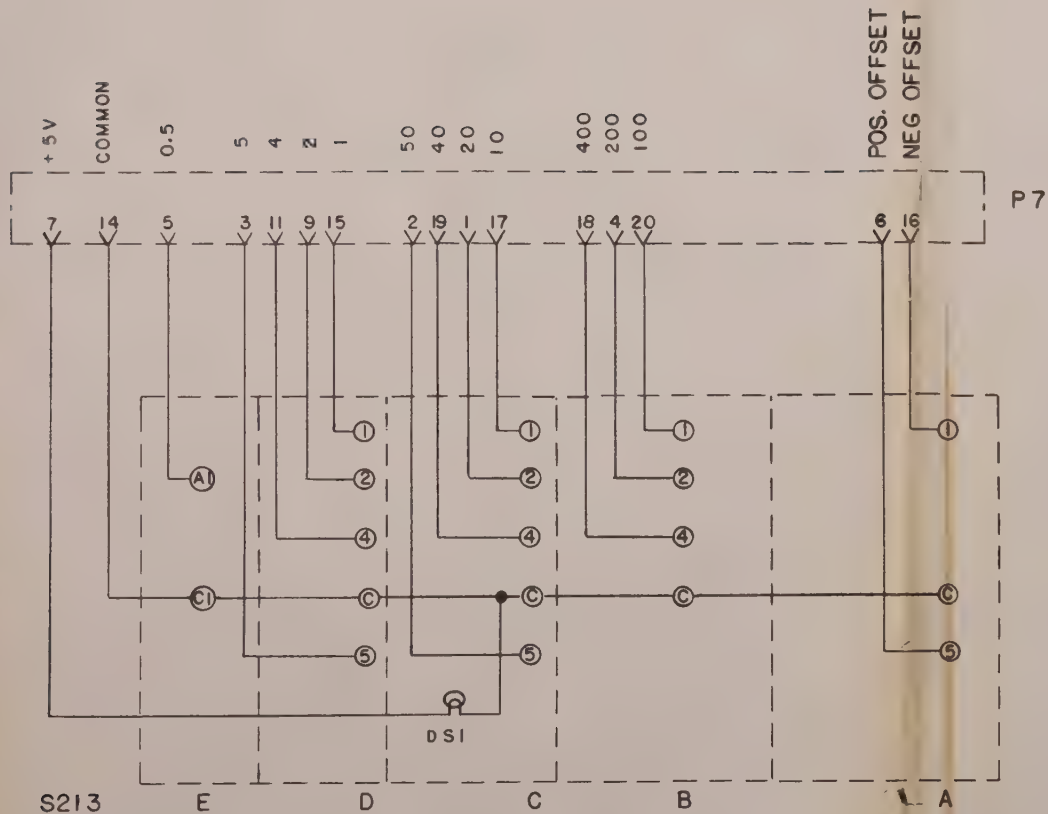
ASS'Y. DWG.
FRONT PANEL INTERFACE BOARD
1501-3



WIRE LIST -702-29938
SW. ASSY 640-29936

SCHEMATIC,
RAMPS SWITCH ASS'Y
(S211)

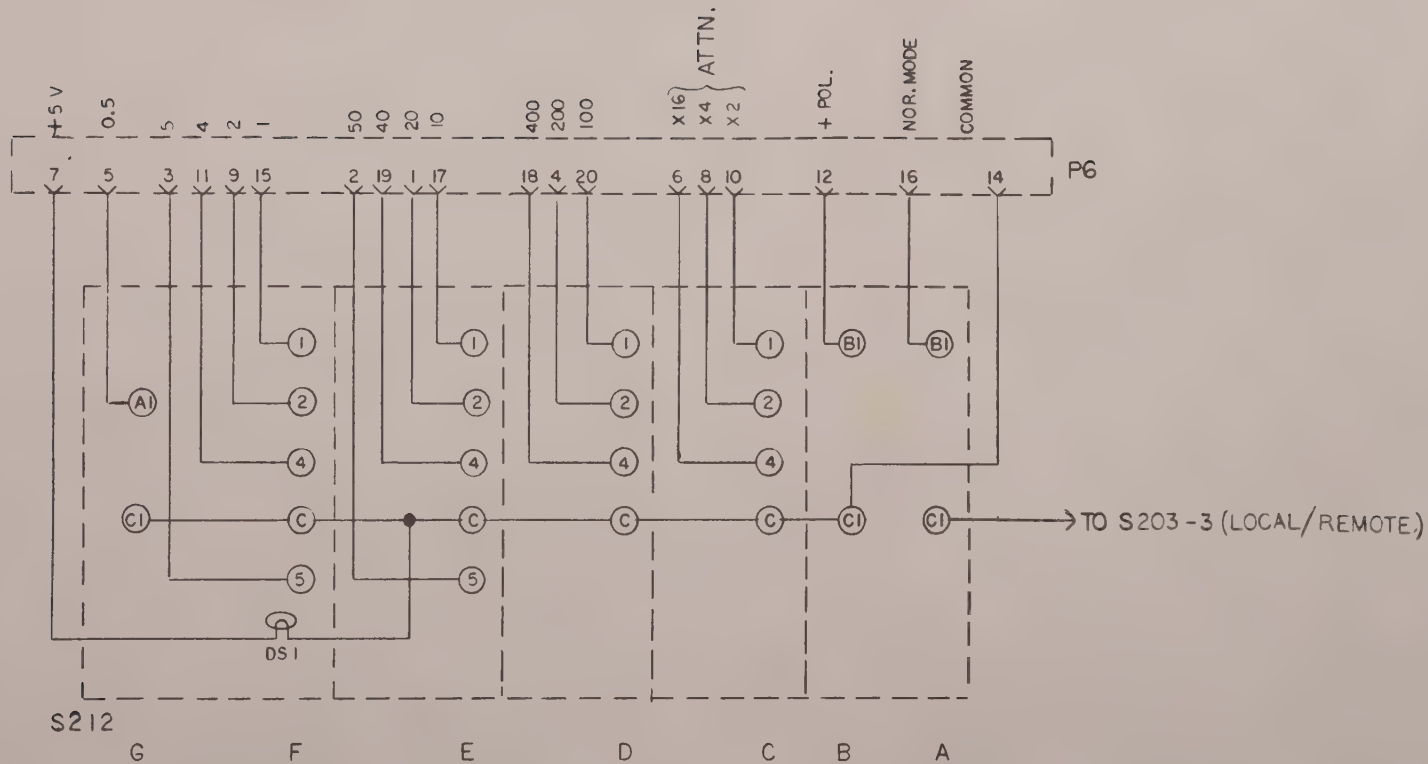
MODEL 1500 SERIES
140-
B-29937 A



SCHEMATIC,
OFFSET SWITCH ASS'Y
(S213)

WIRELIST 702-29941
SW ASSY 640-29939

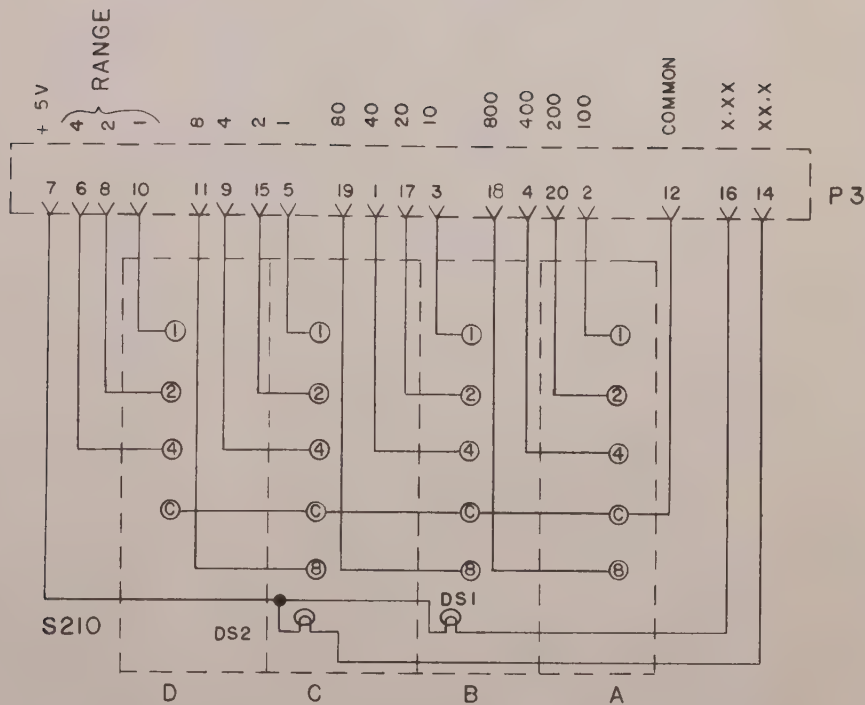
MODEL 1500 SERIES
140-
B-29940
A



SCHEMATIC,
AMPLITUDE SWITCH ASS'Y
(S212)

WIRE LIST 702-29944
SW ASSY 640-29942

MODEL 1500 SERIES
140-
B-29943 A



SCHEMATIC,
WIDTH SWITCH ASS'Y
(S210)

WIRE LIST - 702-29954
SWITCH ASS'Y - 640-29952

MODEL 1500 SERIES

B- 140-29953
A

APPENDIX B-2 PARALLEL

The parallel front panel option is the same as the serial except for the rear panel subassembly. Refer to serial front panel section for the front panel schematic diagrams.

JOB NO.	ASSEMBLIES REQ'D	COST CENTER	DATE

WHERE USED
1501A
1504

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ASSEMBLY NO. 350-21965

COPY DATE 3-28-78

E.C.O. 78-041

DESCRIPTION MOD KIT, PARALLEL PROGRAMMING

GND TRUE/POS TRUE

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A		ADD to INDEX							
B	*401-21212	Parallel D/A Bd Assy	A305-307, A311-314	7					
C									
D		ADD to Rear Panel Assy							
E	*249-21283	Rear Subpanel Assy,							
F		Parallel Prog.		1					
G									
H		ADD to Standard Accessories							
I	700-00024	Connector, 24 Pin Amphenol	P112	1					
J	700-00034	Connector, 50 Pin Amphenol	P110,111	2					
K	146-26326	Documentation List	Prod Ref						
L									
M									
N									
O									
P									
Q									
R									
S									
T									

*SEE 1500 Series

NOTE: MARKETING OPTION 01-PØN/PØP

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

WHERE USED
1500 series
253-21287

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E.C.O. 77-003

ASSEMBLY NO. 249-21283

DESCRIPTION PANEL, SUB, ASSEMBLY

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	248-21194	Panel, Sub		1					
B	706-21374	Cable Assy, 50 Pin	J111	1					
C	706-21284	Cable Assy, 50 Pin	J110	1					
D	706-21285	Cable Assy, 20 Pin	J112	1					
E	144-21195	Silkscreen, Sub Panel	Prod Ref						
F	140-29877	Schematic, Parallel Program	Prod Ref						
G									
H	460-00003	Ground Lug #4 (1)	Prod Ref						
I	201-00004	Screw #3-48x $\frac{1}{2}$ BHMS (6)	Prod Ref						
J	215-00002	Lockwasher #3 (6)	Prod Ref						
K	240-00019	Nut #3-48 (6)	Prod Ref						
L	758-00301	Wire, Bare Buss	Prod Ref	A/R					
M	793-00315	Sleeving, TFE	Prod Ref	A/R					
N									
O									
P									
Q									
R									
S									
T									

TO FRONT PANEL INTERFACE BD (A201)



APPENDIX C-1

OPTION 03
BENCH MOUNT

JOB NO.	ASSEMBLIES REQ'D.	DATE SCHEDULE	DATE

WHERE USED Mult	INDEX ☐	ASSEMBLY ☒	SPEC. ASSEM. ☐	B/M PAGE
	ASSEMBLY NO. 350-21710			COPY DATE 5-11-72
	DESCRIPTION BENCH COMPLETION KIT 5 1/4" X 18"			E.C.O.

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	QTY ASSEM.	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	258-21618	Cover, Top & Bottom		2					
B	258-21559	Side Cover, Left		1					
C	258-21560	Side Cover, Right		1					
D									
E									
F	417-00007	Foot, Black		4					
G									
H									
I									
J		-HARDWARE-							
K	203-00059	Blue Hd #6-32 Screw BHMS (4)	Prod Ref						
L	203-00060	Blue Hd #6-32 FLTHMS Screw (4)	Prod Ref						
M	203-00016	#6-32 Screw FILHMS X 5/8 Lg	Prod Ref						
N									
O									
P									
Q									
R									
S									
T									

DRWN
CHKD REN
APPD _____

APPENDIX C-2

OPTION 04
SLIDE MOUNT KIT

JOB NO.	ASSEMBLIES REQ'D	COST CENTER	DATE

WHERE USED
Mult

INDEX ☐

ASSEMBLY ☒

SPEC. ASSEM. ☐

B/M PAGE _____

ASSEMBLY NO. 350-21764

COPY DATE _____

DESCRIPTION RACK COMPLETION KIT W/SLIDES
5 1/4" X 18"

E.C.O.

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	QTY ASSEM	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	262-21548	Bracket, Rack Mtg Ear		2					
B	258-21555	Cover, Top & Bottom		2					
C	475-21600	Spacer, Slide Mtg		2					
D	*284-16917	Chassis Slide Kit, 20"Std		1					
E									
F									
G									
H									
I		-HARDWARE-							
J	203-00010	FLTHMS 100° #6-32x3/8 Screw	Prod Ref						
K	220-00041	#8-32 Nut-Sert	Prod Ref						
L									
M									
N									
O									
P									
Q									
R									
S									
T									

APPENDIX C-3

OPTION 05
EXTERNAL DRIVE KIT

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

WHERE USED 1500 .MULT	INDEX ☐ ASSEMBLY ☐ SPEC. ASSEM. ☒	B/M PAGE _____ COPY DATE <u>4-30-73</u> E.C.O. <u>77-003</u>
	ASSEMBLY NO. <u>350-21905</u>	
	DESCRIPTION <u>MOD KIT/NO CLOCK EXT DRIVE</u>	

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A		ADD							
B	401-21376	External Clock Drive Assy	J301	1					
C	146-26308	Documentation List	Prod Ref						
D									
E									
F									
G									
H									
I		DELETE							
J	401-19977	Clock Board Assembly	J301	1					
K									
L									
M									
N									
O									
P									
Q									
R									
S									
T									

NOTE: MARKETING OPTION 06

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

WHERE USED
1500 Series

INDEX ☐

ASSEMBLY ☒

SPEC. ASSEM. ☐

B/M PAGE
COPY DATE 7-16-73
E.C.O.

1501A-22

ASSEMBLY NO. 401-21376

DESCRIPTION EXTERNAL DRIVE BOARD ASSEMBLY

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTEN- SION	SHORT
A	400-21375	PC Board		1					
B	401-21376	Assembly Drawing	Prod Ref						
C	140-21377	Schematic	Prod Ref						
D									
E	311-00009	Cap, Cerm 500pf 1KV	C4	1					
F	311-00010	Cap, Cerm .001 μ f 1KV	C6-8	3					
G	311-00041	Cap, Cerm .1 μ f 12V	C3	1					
H	318-00005	Cap, Tant 10 μ f 20V	C1,2,5	3					
I									
J	335-00013	Choke .68 μ h	L2	1					
K	335-00022	Choke 1 μ h	L1	1					
L									
M	374-11731	Diode, 1N751A MP	CR1A&B	1					
N									
O	594-00510	Resistor 51 Ω 1/8W 5%	R2,8	2					
P	595-00100	Resistor 10 Ω 1/2W 5%	R5,7,12,13 26,30,34	7					
Q	595-00102	Resistor 1K 1/2W 5%	R18	1					
R	595-00103	Resistor 10K 1/2W 5%	R27,31,35	3					
S	595-00201	Resistor 200 Ω 1/2W 5%	R10,22,24, 28,32	5					
T	595-00240	Resistor 24 Ω 1/2W 5%	R25,29,33	3					

JOB NO.	ASSEMBLIES REQ'D.	COST CENTER	DATE

WHERE USED
1500 Series

INDEX ☐

ASSEMBLY ☒

SPEC. ASSEM. ☐

B/M PAGE

COPY DATE 7-16-73

E.C.O. 76-050

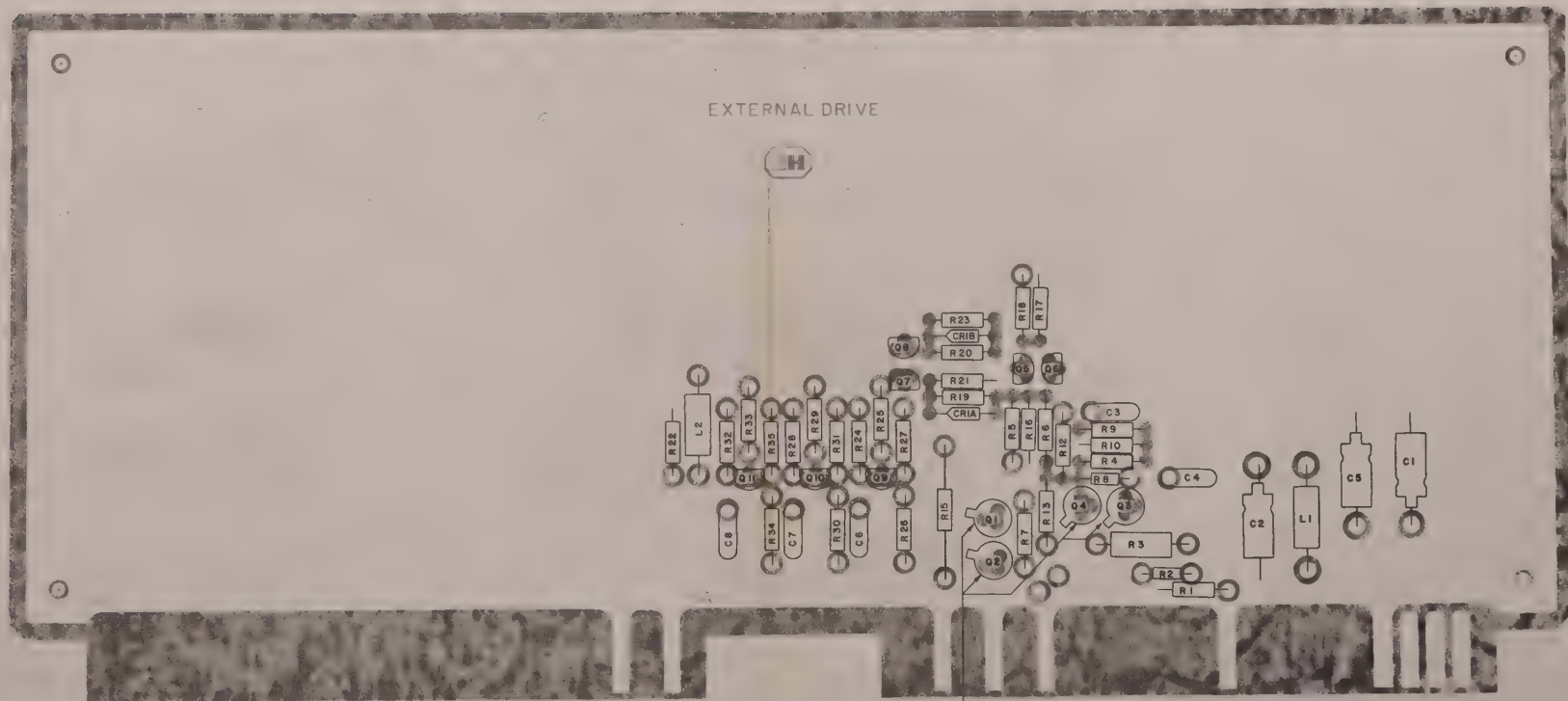
1501A-22

ASSEMBLY NO. 401-21376

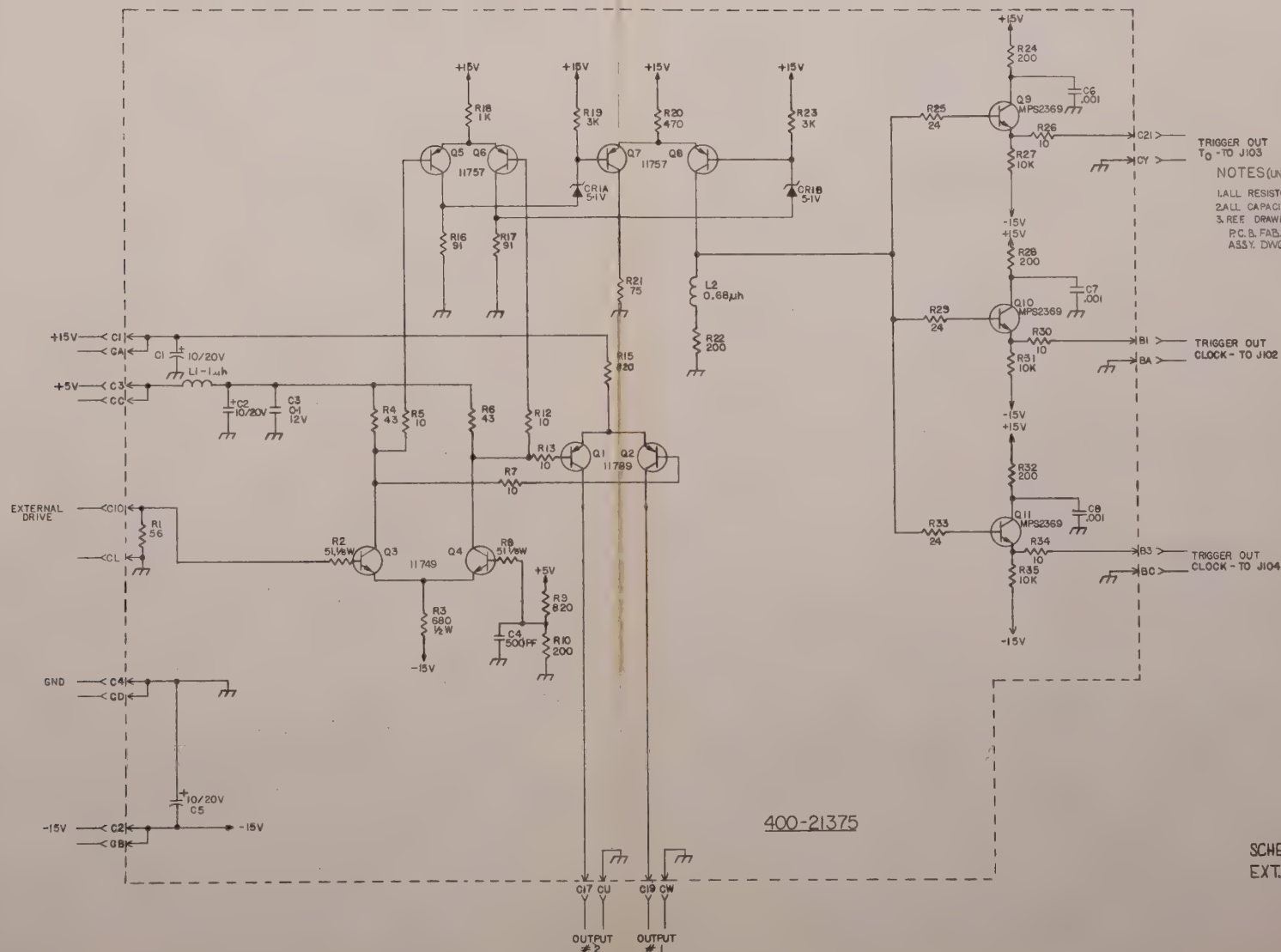
DESCRIPTION EXTERNAL DRIVE BOARD ASSEMBLY

FILLED BY _____ DATE _____ RELEASED TO _____ DATE _____

ITEM	ASSEMBLY OR PART NO.	DESCRIPTION	SCHEMATIC REF.	Q.T. ASSEM.	ISSUED	UNIT COST	UNIT	EXTENSION	SHORT
A	595-00302	Resistor 3K $\frac{1}{4}$ W 5%	R19,23	2					
B	595-00430	Resistor 43 Ω $\frac{1}{4}$ W 5%	R4,6	2					
C	595-00471	Resistor 470 Ω $\frac{1}{4}$ W 5%	R20	1					
D									
E	595-00560	Resistor 56 Ω $\frac{1}{4}$ W 5%	R1	1					
F	595-00750	Resistor 75 Ω $\frac{1}{4}$ W 5%	R21	1					
G	595-00821	Resistor 820 Ω $\frac{1}{4}$ W 5%	R9, 15	2					
H	595-00910	Resistor 91 Ω $\frac{1}{4}$ W 5%	R16,17	2					
I	596-00681	Resistor 680 Ω $\frac{1}{2}$ W 5%	R3	1					
J									
K									
L									
M	663-00112	Transistor MPS 2369	Q9-11	3					
N	663-11749	Transistor	Q3,4	2					
O	663-11757	Transistor	Q5,6,7,8	4					
P	663-11789	Transistor	Q1,2	2					
Q									
R	490-00041	Transistor Pad To-18	XQ1-4	4					
S	495-00027	Amp Pins	XQ1-4	12					
T									



3 AMP PINS (495-00027) &
 1 TRANSISTOR PAD (490-00041)
 UNDER EACH TRANSISTOR.



NOTES (UNLESS OTHERWISE SPEC.)
 1. ALL RESISTORS ARE IN OHMS, $\frac{1}{4}$ W, 5%
 2. ALL CAPACITORS ARE IN μ F
 3. REF. DRAWINGS
 P.C.B. FAB. 400-21375
 ASSY. DWG. 401-21376

SCHEMATIC: P.C.B.
 EXT. DRIVE BD.

1501A
 140-
 21377 B

APPENDIX D

ADDENDUMS

ADDENDUM 1

OLDER MODEL 1501A
WITH EARLIER VERSION OF
WIDTH AND DELAY BOARD
(S/N 21365 and below)

This addendum provides description parts lists, board drawings and schematics for units made before approximately July 1978. These units have an earlier width and delay module.

Sections 1 through 4 of the basic manual apply to these units as well as to other units.

I DESCRIPTION (Width and Delay Module)

The input signal to the width and delay module is supplied to the bases of current mode gating stage Q22, Q23, and Q24 via zener diodes CR4A and CR4B. When a gating signal is applied to the gate input, the flip-flop which is made up of two of the gates of IC3, toggles on the clock pulse to provide a coherent gate signal to the gating transistor Q24. Q24 is biased to remove current from the emitters of Q22 and Q23 and disables the stage. When the input signal returns to ground, Q24 is returned to a normal high state and cuts off. The current is then rerouted to the current mode amplifier, Q22 and Q23. The output of this stage drives coaxial clipping lines CL1 and CL2 to provide a 5 nanosecond spike on each transistion of the input signal. The positive pulse from transistor Q23 and the negative pulse from transistor Q22 are used to drive the delay one-shot. To maintain proper circuit and clipping line action, the unused pulses from these collectors are terminated in resistors R74 and R75.

The delay one-shot consists of transistors Q25, Q26, and Q27 and their associated circuitry. This multivibrator operates in the following fashion. Normally transistors Q27 and Q26 are on and transistor Q25 is off. The collector potential of Q27 is determined by the negative lamp diode, CR3. When the gating amplifier provides a trigger pulse to the one-shot transistor, Q25 turns on and Q26 and Q27 are turned off. The collector potential of Q27 then rises to the positive clamp potential set by CR2.

The emitter of transistor Q26 is provided with a capacitance to ground and with a positive current source. This current source charges the emitter capacitor of this transistor in

a positive direction until transistor Q26 begins to turn on. This action again turns transistor Q27 on and regeneratively drives transistor Q26 so that the timing capacitor in the emitter of Q26 is discharged rapidly through clamping diode CR13. Once the timing capacitor is recharged, the one-shot is back in its normal rest condition ready to be triggered again.

The delay vernier control provides the reference voltage for positive clamp CR2 via the transistor buffer amplifier chain Q17, Q18, and Q19. Varying this bias voltage to the positive clamp diode determines the change in voltage of the timing capacitors and hence the period of the one-shot. Since we are programming the change in voltage to a capacitor, we are in effect directly controlling the period of the one-shot. The 8 ranges of this one-shot are provided by capacitors C8, C25, C26, C27, and C42 and by varying the charging current source transistor Q10.

The ranging circuit operates in the following manner. A range input is supplied to the 1 of 8 decoder, IC2, which in turn activates the transistor switches to turn on the appropriate timing capacitors and controls the current source for the timing capacitors. In the shortest delay range, none of the programmable timing capacitors are activated. Hence, C8 is the only timing capacitor in the circuit while transistor Q7 is saturated. Approximately 10 milliamps of charging current is available to the timing capacitor during this time. In the next lower range, 100 nanoseconds to 1 microsecond, pin 2 of IC2 goes to a logical 1 state which turns on transistors Q57 and Q55 and switching transistor Q56, which connects the timing capacitor, C27 to ground. On the next range down, pin 2 goes to a logical 0 and pin 3 becomes a logical 1. This in turn saturates switching transistor Q42, which connects timing capacitor, C25 to ground. In the 10 microsecond range, the next range down, pin 4 becomes a logical 1 with all other pins at logical 0, which again activated switching transistor Q42, thus connecting capacitor C25 to ground and also supplies a logic 1 to the input of IC1 producing a logic 0 at the output pin 3 of IC1. This high logic level causes transistor Q7 to be cut off reducing the timing current by a factor of 10. Transistor Q28 is also cut off, reducing the bias current to the one-shot. This causes an approximate decade step in the time required to charge capacitor C25. The error term generated is due to the change in bias current to the timing transistor. This is corrected by the current supply to R137, and to the base of transistor Q20, the bias source for the negative clamp. The 100 microsecond to 1 millisecond range is generated when the input causes pin 13 to become a logical 1. With this input low, timing capacitor C26 is activated, and the charging current to the timing capacitor by a factor of 10 while maintaining capacitor C26 active in the circuit. On the 10 ms - 100 ms range, C42 is activated and the charging current is 10 milliamps. On the 100 ms - 1 s range, the charging current is reduced by a factor of ten.

(1) Delay Buffer Amplifier

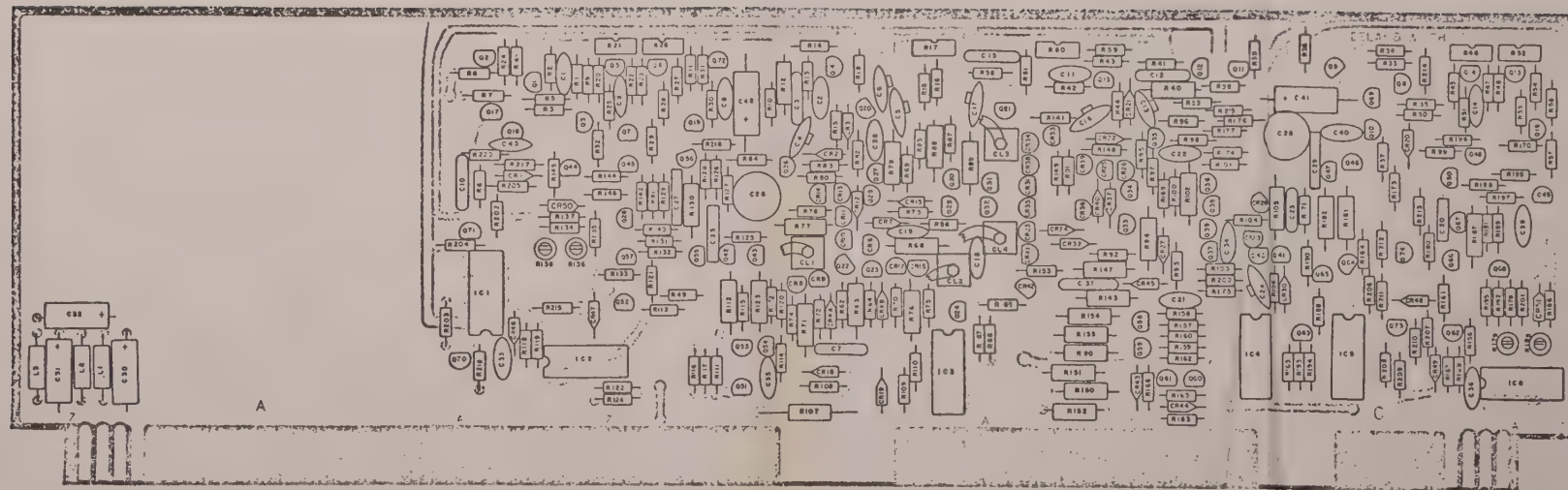
The output of the delay one-shot is coupled via NPN current mode pair Q29 and Q30 to the bases of the current mode pair, Q31 and Q32, whose collectors are differentiated in clipping lines CL3 and CL4 and provide the appropriate drive pulses for the OR gate.

The single pulse/double pulse OR gate always supplies drive pulses to the width one-shot via diodes CR23, CR24, CR38, CR39 and CR40. This pair of signals provides a drive pulse to the width one-shot at the end of each delay interval. In the double pulse mode, diodes CR31, CR32, CR35, CR36, and CR37 also supply pulses to the width one-shot. This OR gate is so designed and controlled that it always provides an approximate 91-ohm terminating resistor for the clipping lines. This provides a 5 ns wide pulse at the input of the OR gate under all operating conditions.

(2) Width One-Shot

The width one-shot consists of transistors Q33, Q34, Q35 and their associated circuitry. This circuit operates in exactly the same fashion as does the delay one-shot and will not be discussed in any further detail.

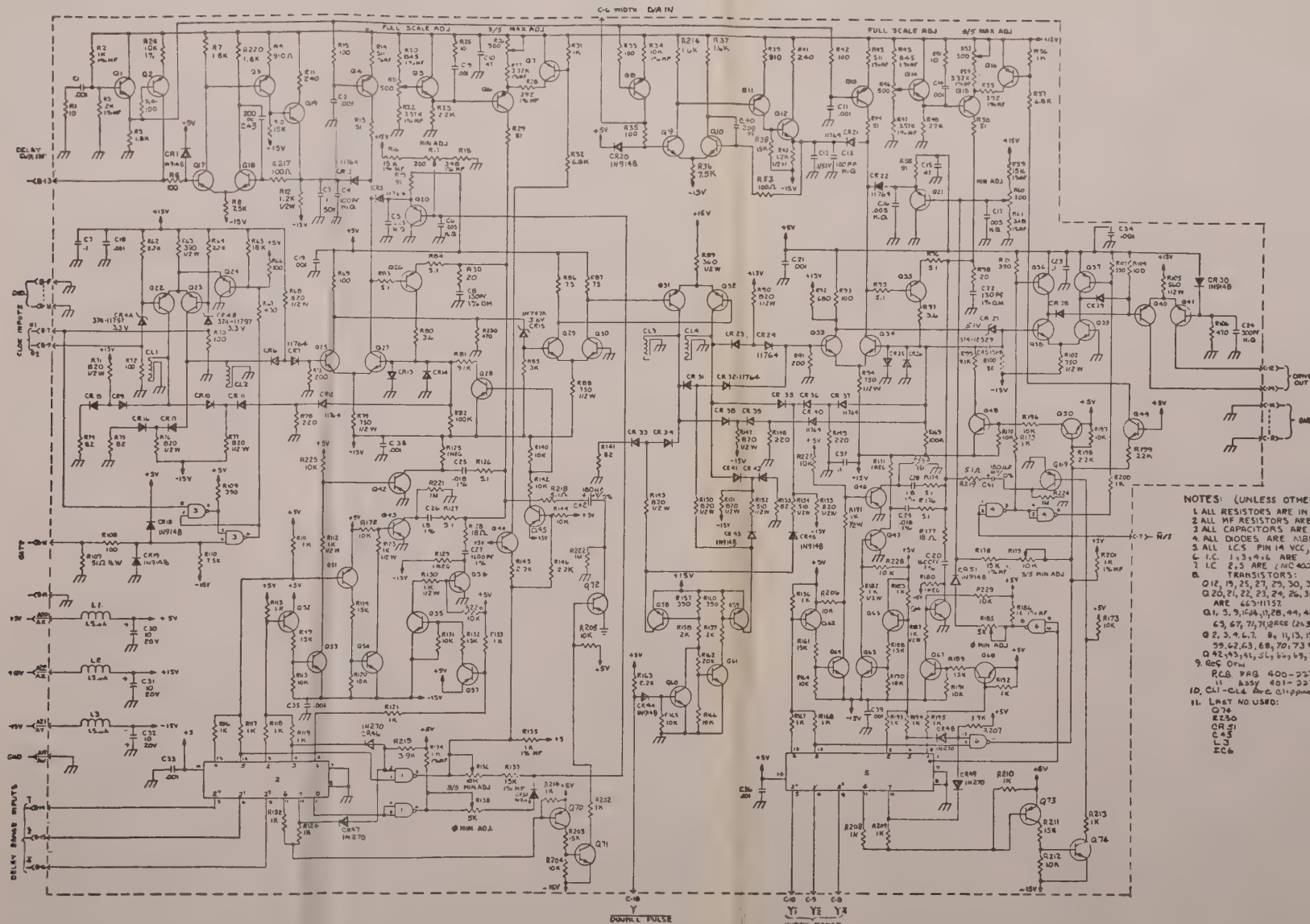
The output of the width one-shot drives current mode pair Q38 and Q39. As a function of the normal/inverted control line (pin C7), either transistor Q36 or Q37 is saturated. The saturated transistor shorts the current mode pair collector to the +5 V supply eliminating the output signal from this source. The other transistor is cut off and allows the signal from its collector to be coupled to the base of the output buffer Q40 and Q41. This signal is amplified by the buffer stage and drives a balanced 50-ohm transmission line system to the output board. When the normal/inverted line is placed in the opposite state, the opposite collector of the current mode pair, Q38 and Q39, is connected to the base of the output drive pair.



ASS'Y. DWG.
DELAY & WIDTH BOARD

1501- A

D- 401-22373



NOTES: (UNLESS OTHERWISE NOTED)

1. ALL RESISTORS ARE IN OHMS, 1% 1/4 W, 5%, CARBON.
2. ALL MF RESISTORS ARE 1/2 W.
3. ALL CAPACITORS ARE IN μ F.
4. ALL DIODES ARE 1N50-101.
5. ALL L.C.S. PIN 14 VCC, PIN 7 GND.
6. I.C. 1, 3, 4, 6 ARE MC 3004P.
7. I.C. 2, 5 ARE (MC 4026B).
8. TRANSISTORS:
 - Q12, 19, 25, 27, 29, 30, 33, 34, 38, 43 ARE MPS-2369
 - Q20, 21, 22, 23, 24, 26, 31, 32, 33, 34, 37, 40, 41 ARE 6C7-1152
 - Q1, 5, 9, 10, 11, 12, 14, 44, 48, 49, 53, 54, 55, 60, 61, 64, 65, 67, 71, 72 ARE (2N3904)
 - Q2, 3, 4, 6, 7, 8, 11, 13, 15, 16, 45, 50, 51, 52, 57, 58, 59, 62, 63, 68, 70, 73 ARE (2N3906)
 - Q42, 43, 44, 45, 46, 47, 49, 51, 52, 53, 72, 47 ARE (2N4403)
 - 9. 60C Dru
 - R.C.B. PRG 400-25272
 - 11. 655V 401-20373
 - 10. C1-C4 ARE C111P40P40MPS
 - 11. LAST NO. USED:
 - Q76
 - R230
 - CR 21
 - C 45
 - L3
 - IC6

SCHEMATIC,
DRIVE & WIDTH BOARD

ADDENDUM 2

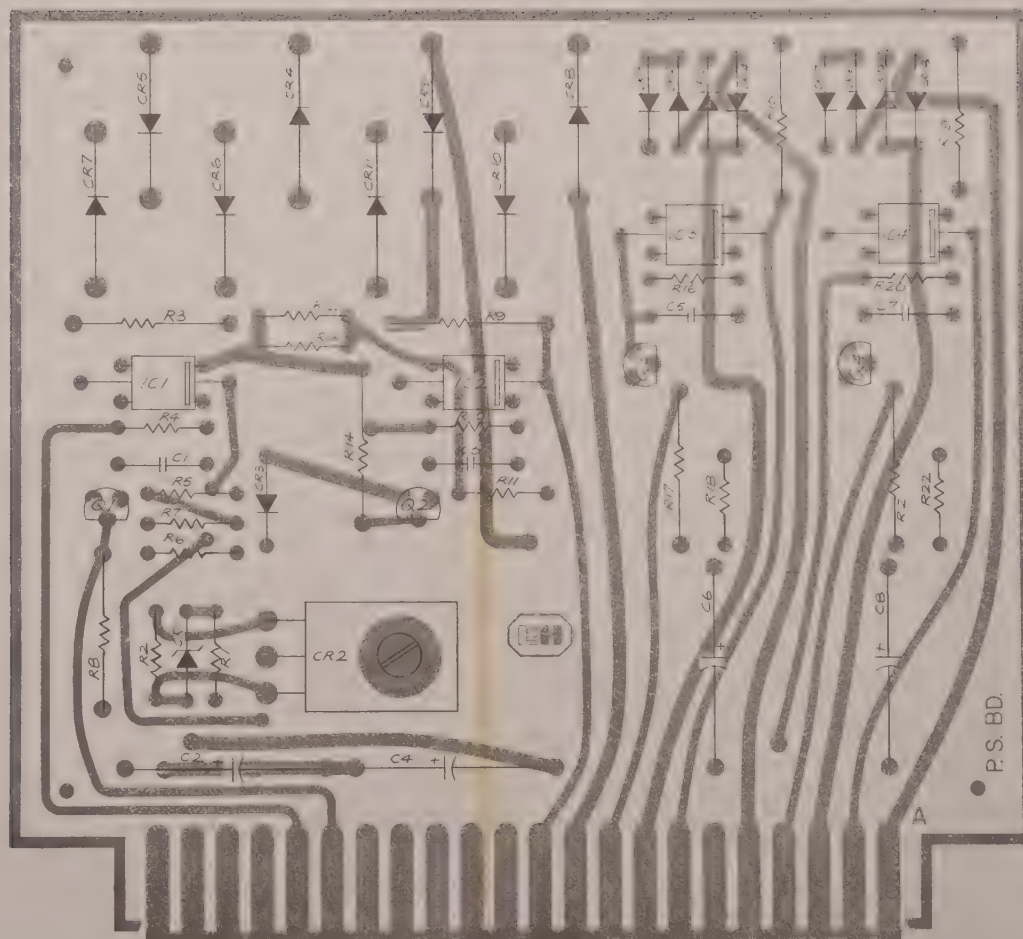
OLDER MODEL 1501A
WITH EARLIER VERSION
OF POWER SUPPLY BOARD
(S/N 19096 and below)

This addendum provides description, parts list, board drawings, and schematics for units made before approximately January 1977. These units have an earlier Power Supply Regulator Board. Section 1 through 4 of the basic manual apply to these units as well as to other units.

I DESCRIPTION (Power Supply)

The E-H Model 1501 Model 1501A utilizes four nearly identical power supplies to supply the analog circuitry and a fifth supply is utilized to deliver the voltage necessary for the logic circuitry. This supply utilizes a fixed reference IC (IC301 which is located on the chassis) and an over voltage and reverse polarity protection circuit which consists of CR1 and CR2, and CR3. The IC regulator is so designed that it automatically protects itself against short circuits. However, if an over-voltage condition exists the SCR CR2 is turned on via zener diode CR1 and its gate circuit, and effectively crow bars the power supply to ground. If for any reason the supply is shorted to the -15 V supply, diode CR 3 clamps the supply to -0.7 V. In either case, the digital IC's within the instrument are protected.

The remaining power supplies are similar to the +15 V supply which consists of IC1, Q304, and the associated circuitry. The output voltage of this supply is sensed by input pin 6 of IC1 at the junction of the voltage divider made up of R1 and the parallel combination of R6 and R7. The magnitude of the voltage at pin 6 with respect to ground is approximately 4 V. This input produces a controlled signal at pin 3 of the IC which drives the base of the series pass transistor, Q304, whose emitter supplies the current for the +15 V supply. Before this current is passed to the supply bus, however, its magnitude is monitored via resistor R8. If the current through this resistor exceeds about 1-1/2 amps, pin 5 of the IC is moved in a negative direction which cuts off the output of IC1 returning off the series pass transistor and limiting the overall current of the supply. A secondary protection loop exists utilizing the internal current sensing capability of this IC via the feedback to pin 4. If the base current of Q304 exceeds 100 mA again, IC1 current limits and shuts down the supply. This supply is set within 1% of its nominal value at the factory and should remain within 1%.



ASSEMBLY DRAWING
POWER SUPPLY BOARD

MODEL 1501
C-401-19756
ISSUE A

COMPONENTS:
 1. ALL RESISTORS
 2. ALL CAPACITORS
 3. ALL TRANSISTORS
 4. I.C. 1-4 ARE 74100, 74101, 74102
 5. REF. DWG. P.C. BD.
 6. PRIMARY FUSION R.6 AND 12 AF

NOTES: UNLESS OTHERWISE SPECIFIED, ALL COMPONENTS ARE TO BE PURCHASED FROM THE FOLLOWING SOURCES:
 1. ALL RESISTORS
 2. ALL CAPACITORS
 3. ALL TRANSISTORS
 4. I.C. 1-4 ARE 74100, 74101, 74102
 5. REF. DWG. P.C. BD.
 6. PRIMARY FUSION R.6 AND 12 AF

1. ALL RESISTORS ARE IN OHMS, 1/4W 5%
2. ALL CAPACITORS ARE IN μ F.
3. ALL TRANSISTORS ARE 2N3804.
4. I.C. 1-4 ARE MFC 6030
5. REF DWG:
P.C. BD. FAB 400-19755
ASSY 401-19756
6. PRIMARY FUSE RATING IS 2 1/2 AMP @ 117 VAC
R6 AND I2 ARE 1% MF.

1501
140-
F- 19757 F

ADDENDUM 3

MODEL 1501A WITH EARLIER
REVISIONS OF SERIAL D/A BOARDS

This addendum provides board drawings and schematics for the different revision Serial D/A boards used in the Model 1501A.

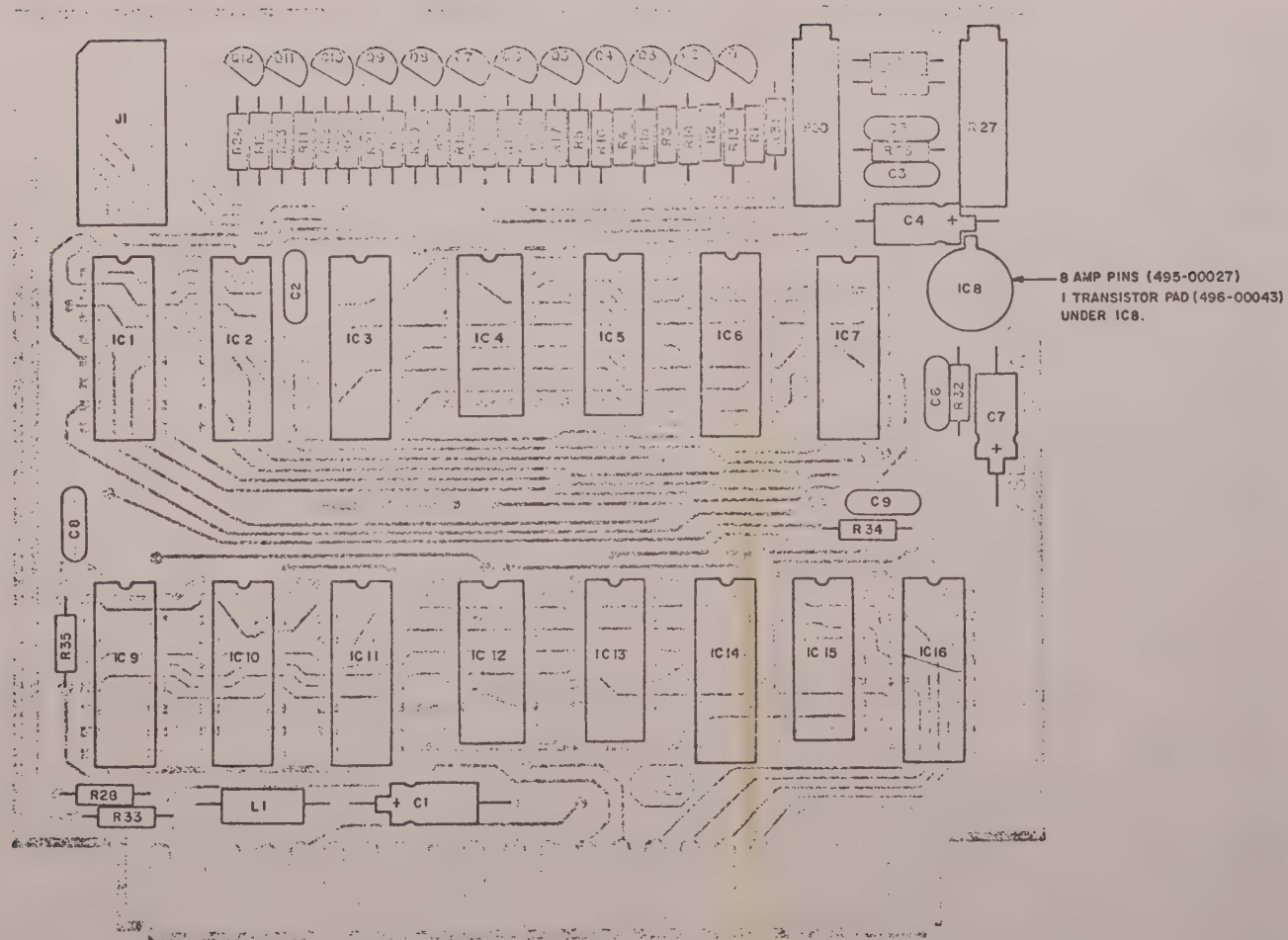
The different revisions D through F are interchangeable into any Model 1501A. The differences are only IC changes, which do not effect the overall performance of the D/A board. The differences are the type of devices used for IC 4, 5, and 12.

When ordering parts please specify part description and board revision designation.

Example: MC3002 Board No. 400-22618D

REVISION CROSS REFERENCE

Board Revision	Schematic Revision
400-22618D	140-22620F
400-22618E	140-22620G
400-22618F	140-22620H

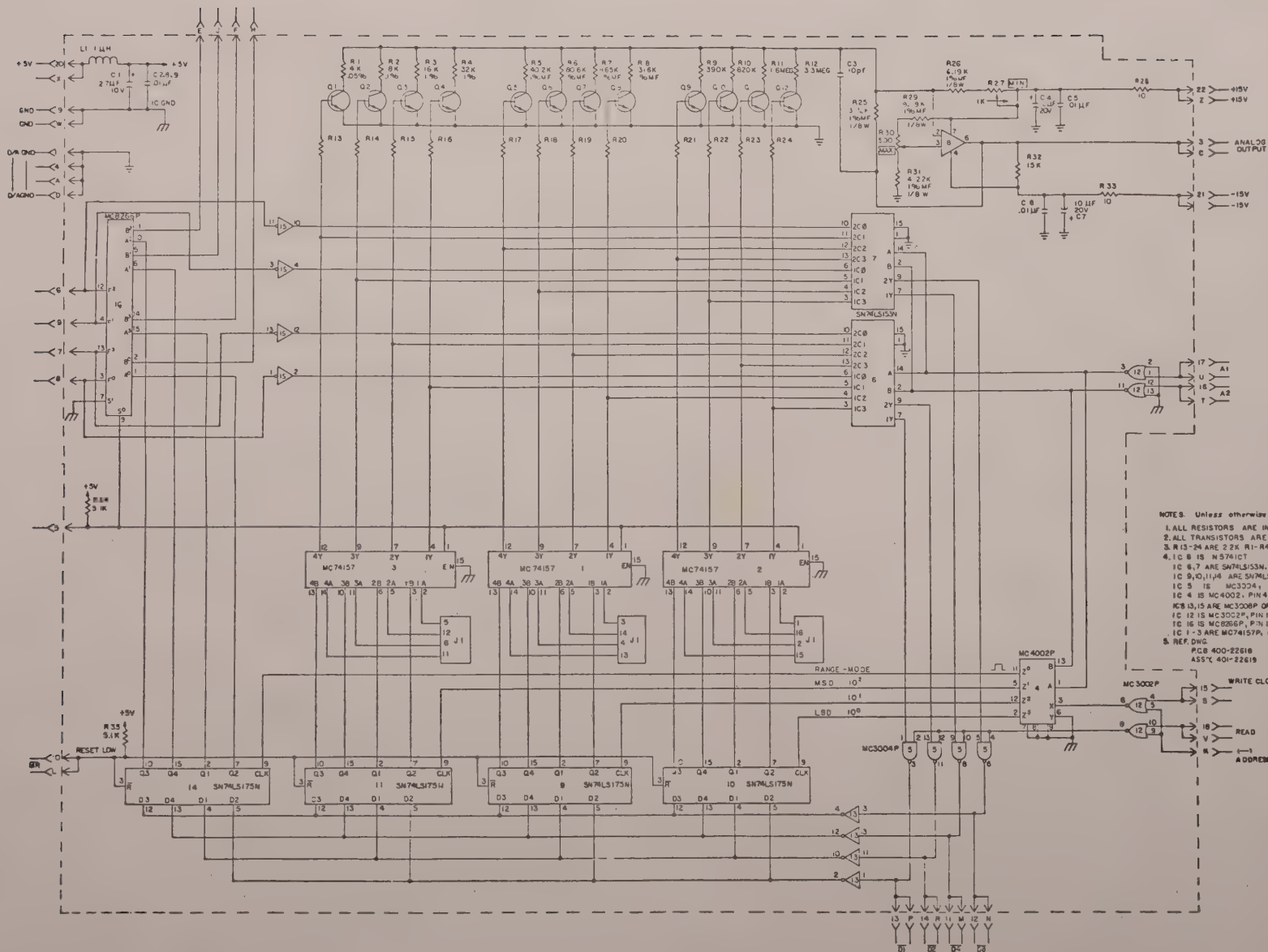


ASSEMBLY, SERIAL D/A BOARD

MODEL NO: 1501A

C- 401-22619

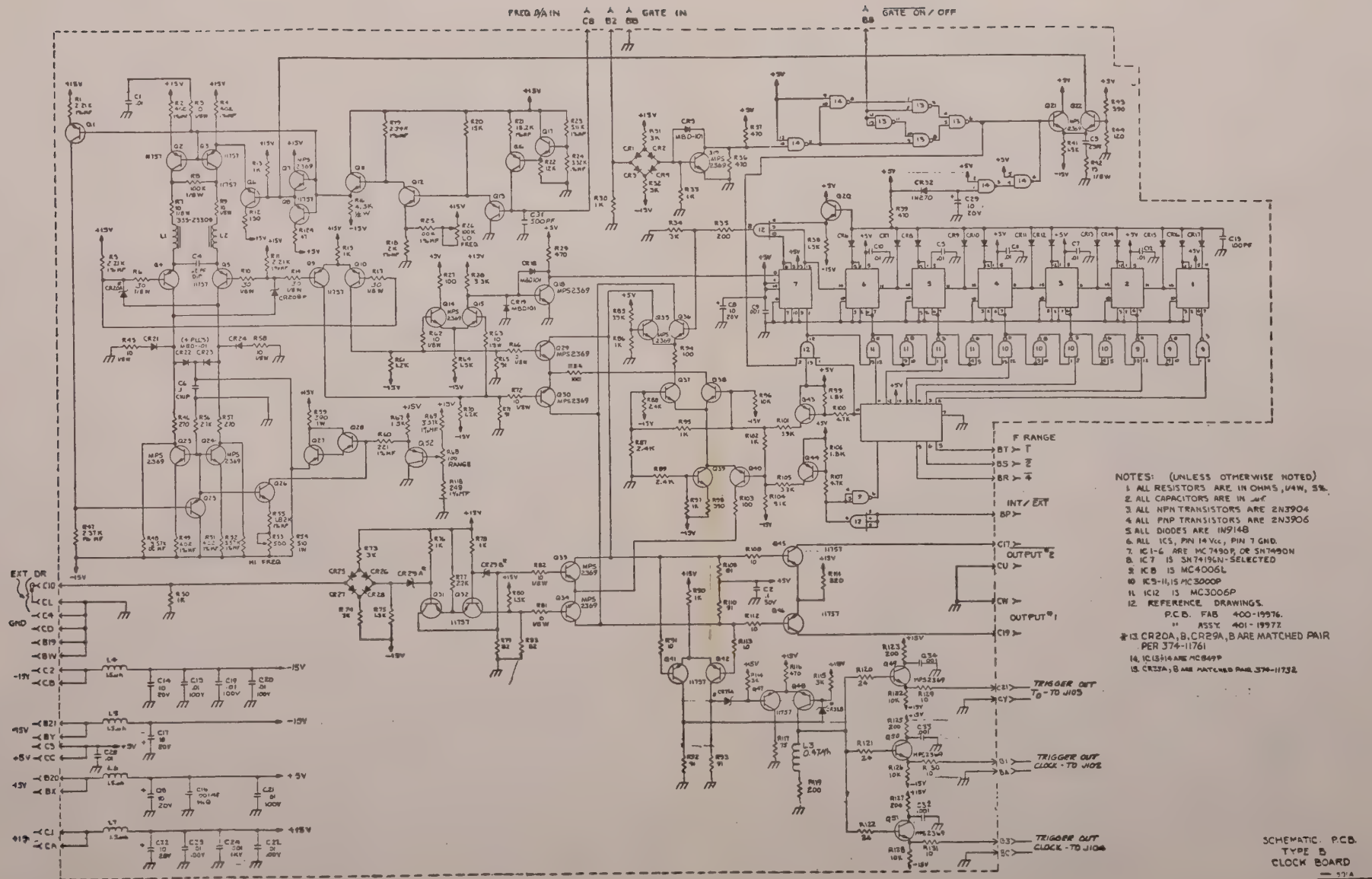
E



- NOTES: Unless otherwise noted
1. ALL RESISTORS ARE IN Ω , $k\Omega$, $M\Omega$, 5%.
 2. ALL TRANSISTORS ARE 2N3904.
 3. R15-24 ARE 22K. R1-R4 ARE VISHAY V53-1.
 4. IC 8 IS MC74157.
 5. IC 9, 7 ARE SN74LS157N. PIN 16 VCC, PIN 8 GND.
 6. IC 9, 10, 11 ARE SN74LS157N. PIN 16 VCC, PIN 8 GND.
 7. IC 5 IS MC3002P. PIN 16 VCC, PIN 7 GND.
 8. IC 4 IS MC4002. PIN 4 VCC, PIN 10 GND.
 9. IC 13, 15 ARE MC3002P OR SN74LS157N. PIN 16 VCC, PIN 7 GND.
 10. IC 12 IS MC3002P. PIN 16 VCC, PIN 7 GND.
 11. IC 16 IS MC8026P. PIN 16 VCC, PIN 8 GND.
 12. IC 1-3 ARE MC74157N. PIN 16 VCC, PIN 8 TO GND.

5. REF. DWG.
PCB 400-22618
ASSY 401-22619

WRITE CLOCK
READ
ADDRESS

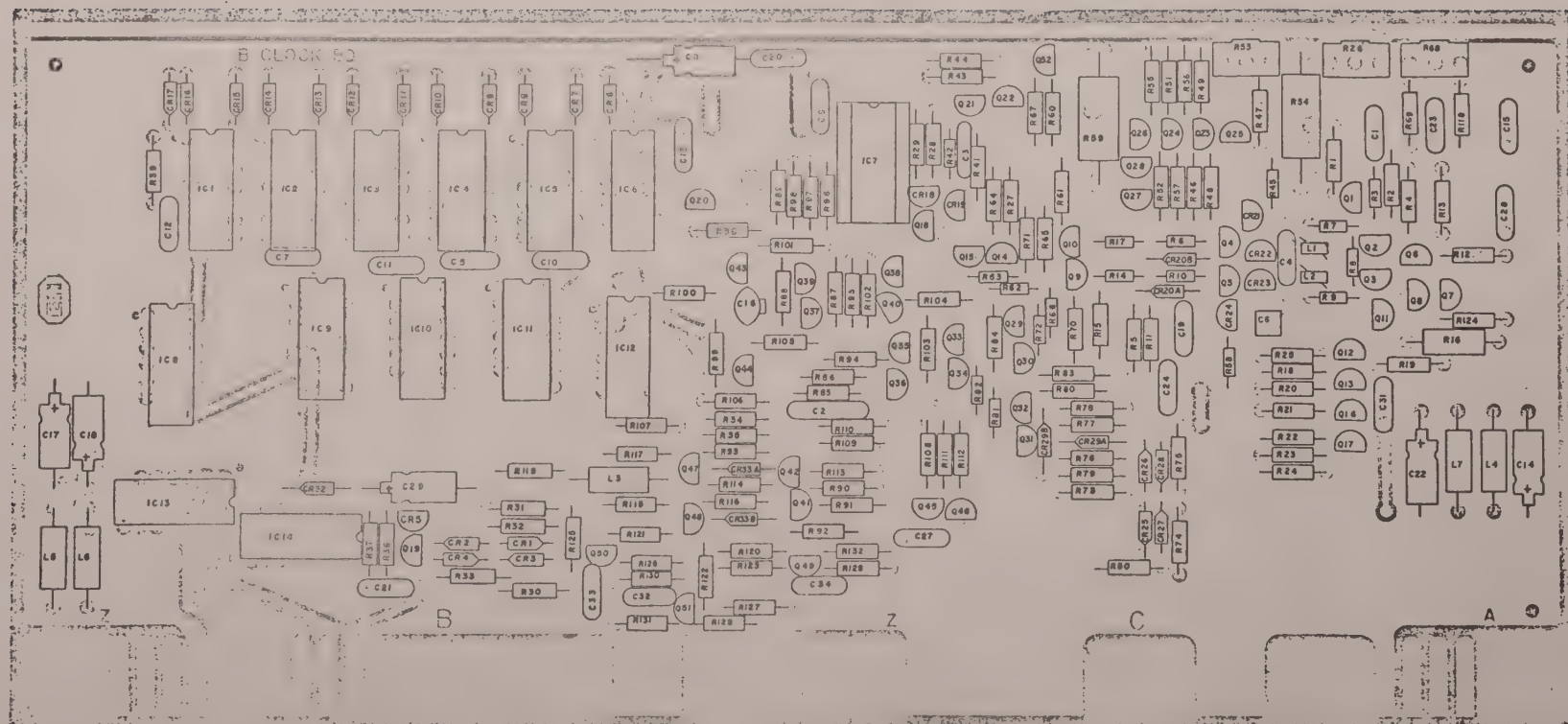


ADDENDUM 4

MODEL 1501A WITH EARLIER
REVISION TYPE B CLOCK BOARDS

This addendum provides board drawings and schematics for the earlier revision clock board.

The revision change was to add Q58 and Q59 for compatibility with the other Model 1500 series units. This change does not have any effect on the Model 1501A, and all revisions A through G are interchangeable in any 1501A.



ASSEMBLY DRAWING
CLOCK BOARD

APPENDIX E

CIRCUIT EQUIVALENTS - INTEGRATED CIRCUITS

The major IC components in the 1501A Programmable Pulse Generator are described in this section to aid in circuit description, troubleshooting and repair of the unit. Components are not described in complete detail but are extracts from the manufacturers' specification catalog.

For those IC's not described or if more significant characteristics are required, refer to the appropriate manufacturer's specification sheet and/or catalog. Table E-1 lists the IC's in alphanumeric manufacturers' part number order.

TABLE E-1. I.C. COMPONENT DESCRIPTIONS

COMPONENT NUMBER	TITLE	E-H PART NUMBER	PAGE
MC1741CG	General Purpose Compensated Single Unit OpAmp	665-00079	E-3
MC3000P	TTL Quad 2-Input Positive NAND Gate	665-00053	E-4
MC3002P	TTL Quad 2-Input NOR Gate	665-00110	E-5
MC3004P	Quad 2-Input NAND Gate	665-00078	E-6
MC3006P	TTL Triple 3-Input AND Gate	665-00062	E-7
MC3007P	TTL Triple 3-Input NAND Gate	665-00114	E-8
MC3022	TTL Quad 2-Input Exclusive NOR Gate	665-00084	E-9
MC3024P	TTL Dual 4-Input NAND Buffer Gate	665-00146	E-10
MC3060P	TTL Dual D Pos Edge-Trig Flip-Flop w/PRST & Clr	665-00056	E-11
MC3061P	TTL Dual J-K Master Slave Flip-Flop with Clear	665-00054	E-13
MC4002P	TTL 32x8 Static ROM	665-00151	E-15
MC4006P	TTL Binary to Octal (1 of 8) Decoder	665-00057	E-16
MC4007P	TTL Dual Binary 1-of-4 Line Gated Decoder	665-00149	E-18
MC4008P	TTL 8-Bit Parity Tree	665-00150	E-20
MC4015P	TTL Quad Flip-Flop	665-00144	E-21
MC4038P	TTL Inverting/Non-Inverting One-of-Eight Decoder	665-00123	E-22
5082-4360	DTL/TTL Compatible Optically Coupled Gate	665-00210	E-23
723	150mA 2V/37V Adjustable Voltage Regulator	665-00164	E-24
7242P	TTL Quad 2-Input Exclusive NOR Gate	665-00154	E-25
MC7266P	TTL Quad 2-Input 4-Bit Multiplexer	665-00152	E-26
7400	TTL Quad 2-Input NAND Gate	665-00024	E-28
74LS00	TTL Quad 2-Input NAND Gate	665-00137	E-28
7401P	TTL Quad 2-Input Positive NAND Gate	665-00094	E-28
74H01	TTL Quad 2-Input Pos NAND Gate Open Collector	665-00172	E-28
7402	TTL Quad 2-Input Positive NOR Gate	665-00050	E-28
7404	TTL Hex Inverter	665-00085	E-29
74LS04	TTL Hex Inverter	665-00334	E-29
7408	TTL Quad 2-Input AND Gate	665-00190	E-30
7410N	TTL Triple 3-Input Positive NAND Gate	665-00025	E-30
7414N	TTL Hex Schmitt Trigger Inverter	665-00237	E-31
7420	TTL Dual 4-Input NAND Gate	665-00088	E-32
7425N	TTL Dual 4-Input NOR with Strobe	665-00148	E-33
7430	TTL 8-Input NAND Gate	665-00090	E-34
7438N	TTL Quad 2-Input NAND Buffer Gate	665-00155	E-35
7442	TTL BCD-To-Decimal Decoder	665-00089	E-36
7474	TTL Dual D-Type Flip-Flop	665-00197	E-37
7485N	TTL 4-Bit Amplitude Comparator	665-00198	E-38

TABLE E-1. I.C. COMPONENT DESCRIPTIONS (Cont'd)

COMPONENT NUMBER	TITLE	E-H PART NUMBER	PAGE
7486N	TTL Quad 2-Input Exclusive OR Gate	665-00189	E-39
74LS86	TTL Quad 2-Input Exclusive OR Gate	665-00383	E-39
7490	TTL Decade Counter	665-00076	E-40
74123N	TTL Dual Retriggerable Monostable Multivibrator	665-00139	E-41
74S133	TTL 13-Input NAND Gate	665-00140	E-42
74LS138	TTL 3-Line to 8-Line Decoder/Demultiplexer	665-00369	E-43
74145	CMOS Counter/Divider 7-Stage Ripple Counter	665-00080	E-44
74LS153	TTL Dual 4-Line To 1-Line Data Slctr/Mltplxr	665-00339	E-45
74157	TTL Quad 2-Input Multiplexer	665-00153	E-46
74175	TTL Hex Quad D Edge-Triggered Flip-Flop	665-00183	E-47
74LS175	TTL Quad D Type Flip-Flop	665-00341	E-47
74196N	0-50 & 0-25 MHZ Presettable Decade Counter/Latch	665-00077	E-49
75452P	Dual Peripheral NAND Driver	665-00133	E-50
75453P	Dual Peripheral OR Driver	665-00100	E-50
8309P	TTL Dual 4-Input Multiplexer Comp Output	665-00145	E-51

MC1741CG

665-00079

INTERNALLY COMPENSATED, HIGH PERFORMANCE
OPERATIONAL AMPLIFIERS

... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Low Noise Selections Offered - N Suffix

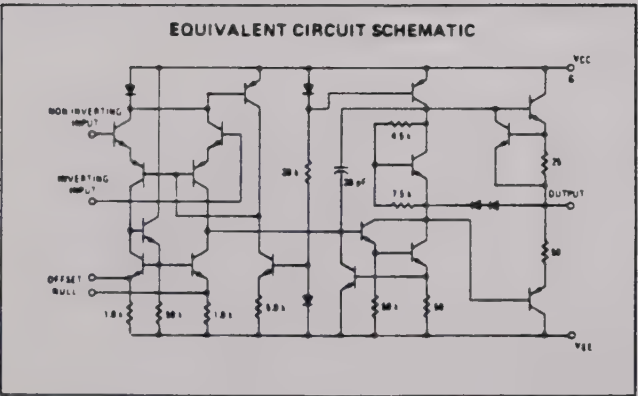
MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted)

Rating	Symbol	MC1741C	MC1741	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc Vdc
Input Differential Voltage	V_{ID}	± 30		Volts
Input Common Mode Voltage (Note 1)	V_{ICM}	± 15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70 -55 to +125		$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150		$^{\circ}\text{C}$
Junction Temperature Range	T_J	175 150		$^{\circ}\text{C}$

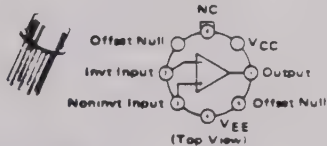
Note 1 For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage

Note 2 Supply voltage equal to or less than 15 V

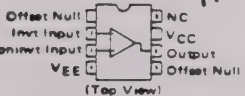
EQUIVALENT CIRCUIT SCHEMATIC



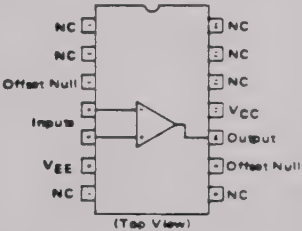
G SUFFIX
METAL PACKAGE
CASE 601



P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1741C, MC1741NC)



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-118



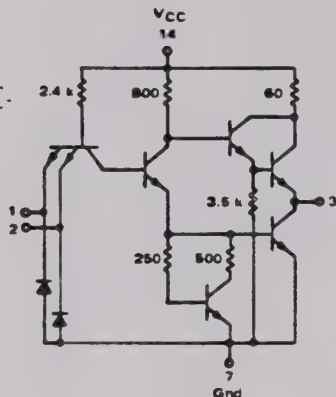
F SUFFIX
CERAMIC PACKAGE
CASE 806 04
TO 91



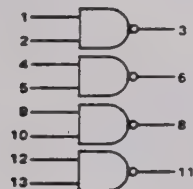
TTL QUAD 2-INPUT POSITIVE NAND GATE

MC3000P

665-00053

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN

This device consists of four 2-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.



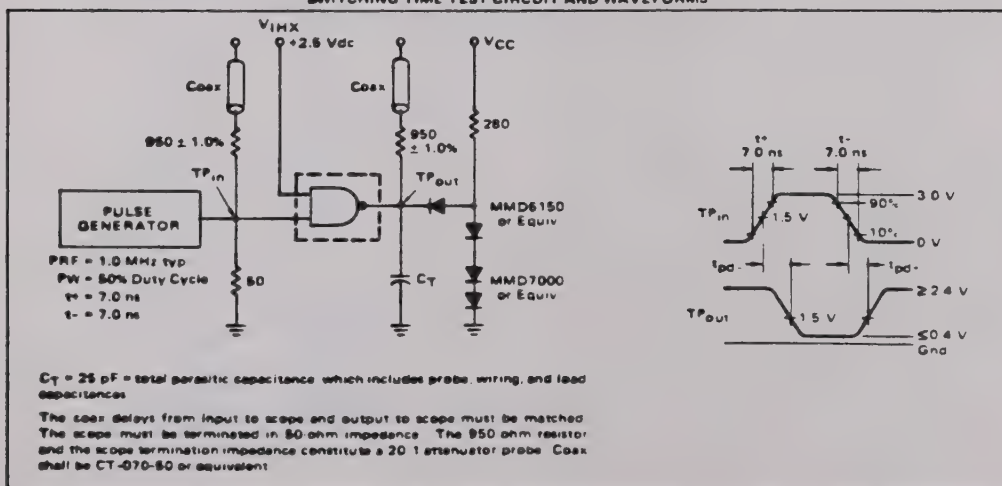
Positive Logic: $3 = 1 \cdot 2$
Negative Logic: $3 = 1 + 2$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 88 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

Pin numbers for the 54H00F/74H00F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3100F/L/3000F/LP	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H00F/74H00F	1	2	3	6	7	5	11	8	9	10	14	12	13	4

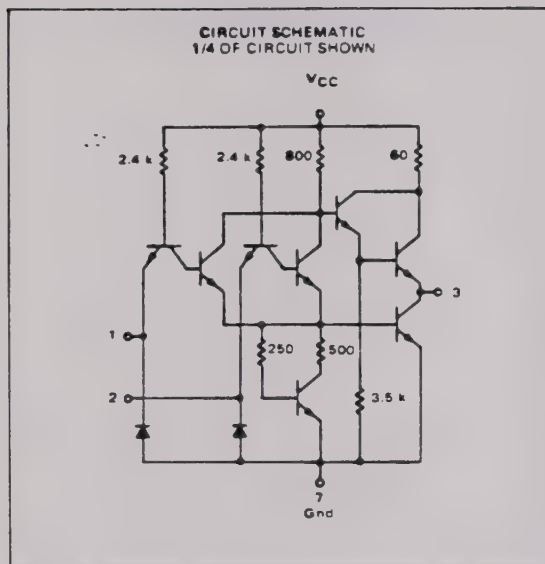
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



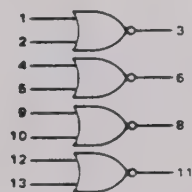
TTL QUAD 2-INPUT NOR GATE

MC3002P

665-00110



This device consists of four 2-input NOR gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.

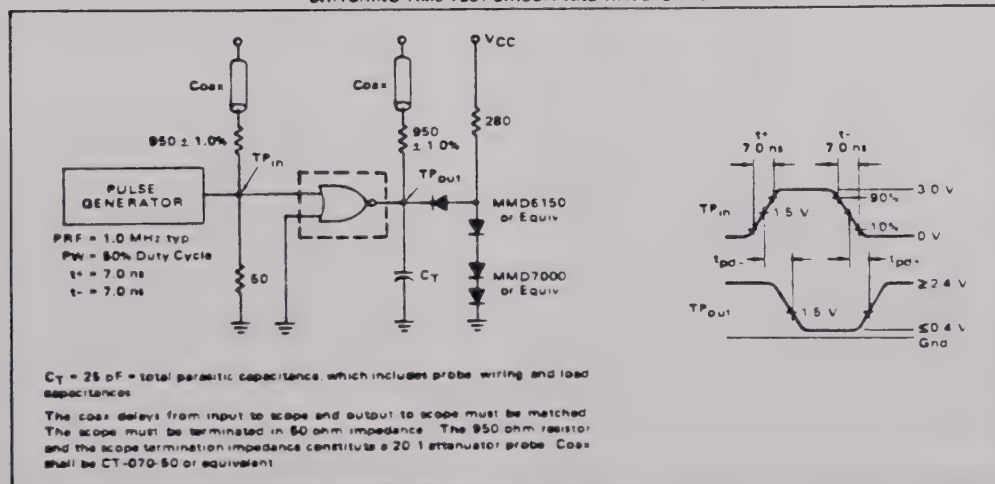


Positive Logic $3 = \overline{1 \cdot 2}$

Negative Logic $3 = \overline{1} \cdot \overline{2}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 122 mW typ pkg
Propagation Delay Time = 6.0 ns typ

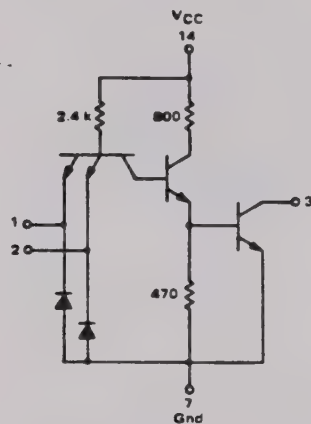
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



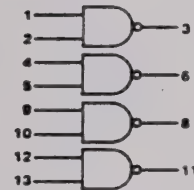
TTL QUAD 2-INPUT NAND GATE

MC3004P

665-00078

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN

This device consists of four 2-input NAND gates with no output pull-up circuits. It can be used where the Wired-OR-function is required or for driving discrete components.



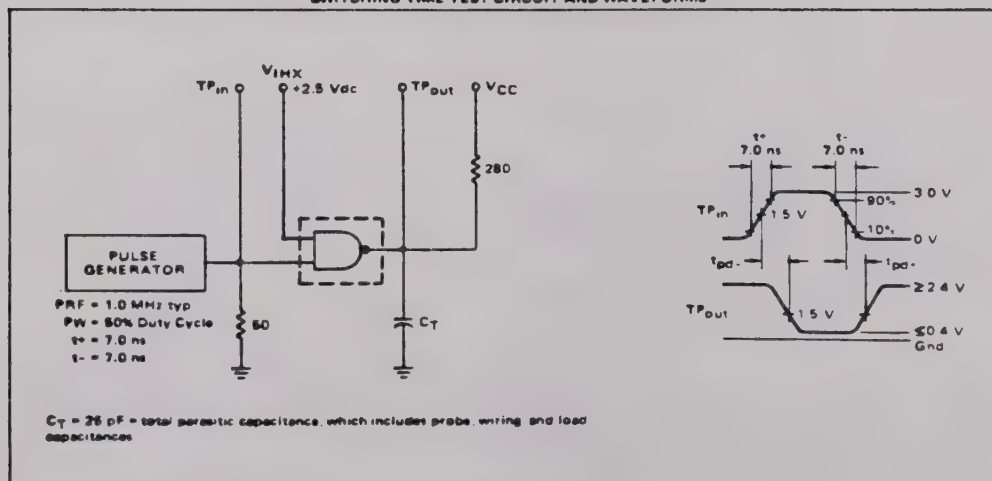
Positive Logic $3 = \overline{1 \cdot 2}$
Negative Logic $3 = \overline{1} \cdot \overline{2}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 88 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

Pin numbers for the 54H01F/74H01F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3104F.L/3004F.L.P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H01F/74H01F	1	2	3	6	7	5	11	8	9	10	14	12	13	4

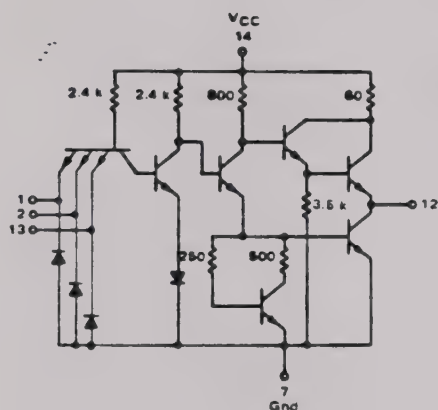
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



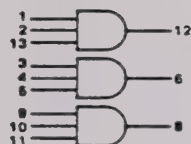
TTL TRIPLE 3-INPUT AND GATE

MC3006P

665-00062

CIRCUIT SCHEMATIC
1/3 OF CIRCUIT SHOWN

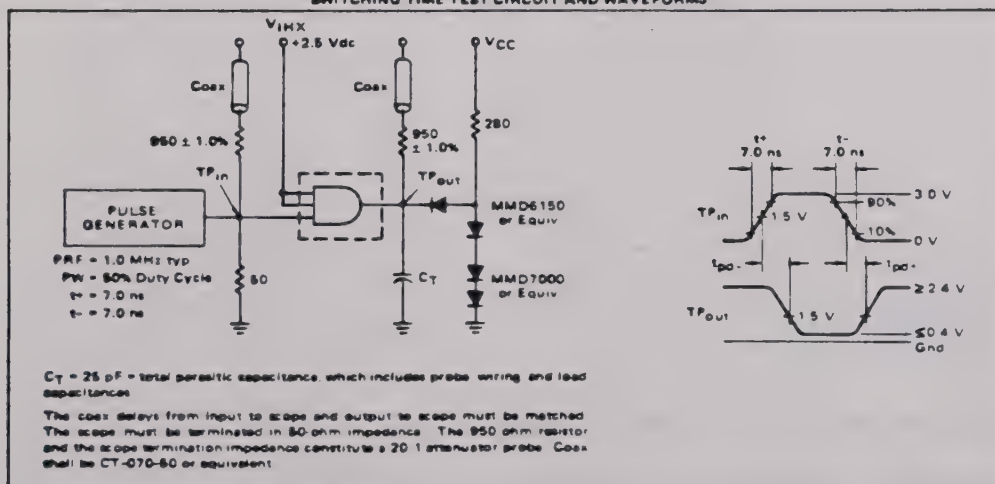
This device consists of three 3-input AND gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.



Positive Logic: $12 = 1 + 2 + 13$
Negative Logic: $12 = 1 + 2 + 13$

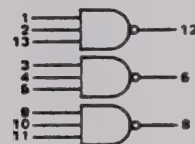
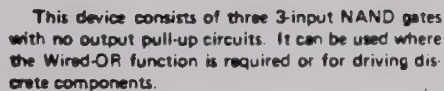
Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 84 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC3007P

665-00114



Positive Logic: $12 = \overline{1 + 2 + 13}$
Negative Logic: $12 = \overline{1 + 2 + 13}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 66 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

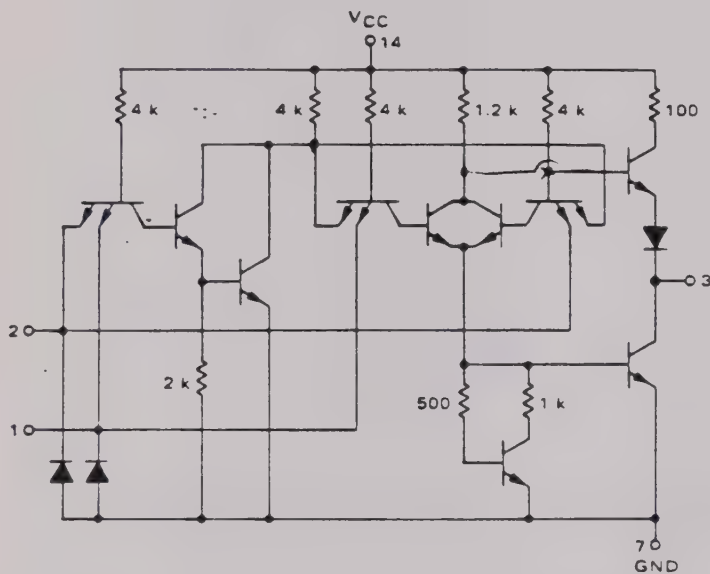
Figure 1 shows the timing diagram and circuit schematic for the 74VHC00. The schematic includes a pulse generator connected to the input of the 74VHC00 inverter. The input is labeled TP_{in} and the output is labeled TP_{out} . The input voltage is $V_{IH(X)} = 2.5 \text{ Vdc}$. The output is connected to V_{CC} through a 280Ω resistor and to ground through a capacitor C_T . The timing diagram shows the input and output waveforms. The input waveform has a rise time $t_{r+} = 7.0 \text{ ns}$, a fall time $t_{f-} = 7.0 \text{ ns}$, and a pulse width $t_p = 1.5 \text{ V}$. The output waveform has a rise time $t_{r+} = 7.0 \text{ ns}$, a fall time $t_{f-} = 7.0 \text{ ns}$, and a pulse width $t_p = 1.5 \text{ V}$. The output voltage is $V_{OH} = 3.0 \text{ V}$ and $V_{OL} = 0.4 \text{ V}$.

TTL QUAD 2-INPUT EXCLUSIVE NOR GATE

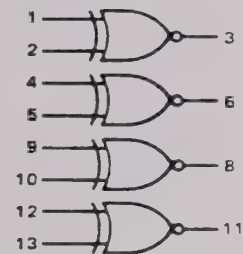
MC3022

665-00084

1/4 OF CIRCUIT SHOWN



This device consists of four 2-input Exclusive NOR gates. They can be used to build parity checking/generating functions. Up/down counters can be built using these gates and J-K flip-flops.



Positive Logic: $3 = \overline{1} \cdot \overline{2} + 1 \cdot 2$

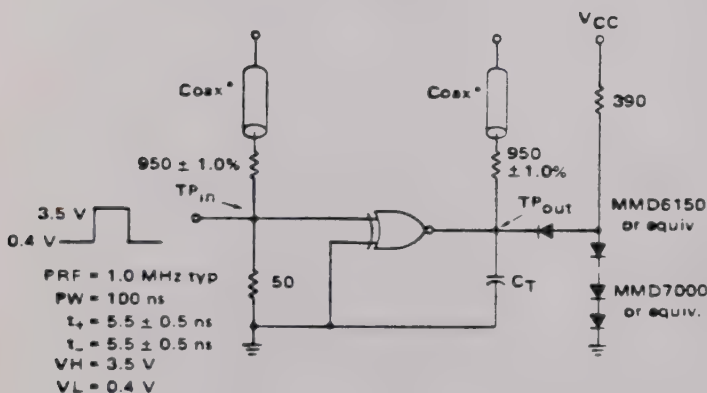
Input Loading Factor = 1.6

Output Loading Factor = 8

Total Power Dissipation = 85 mW typ/pkg

Propagation Delay Time = 14 ns typ

SWITCHING TIME TEST CIRCUIT

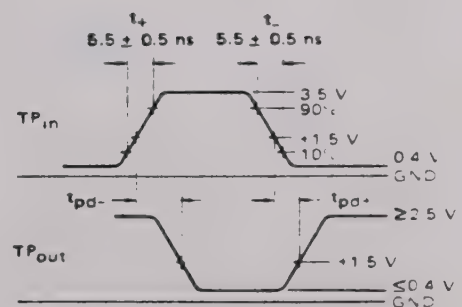


*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50 ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

Ground inputs of gates not under test

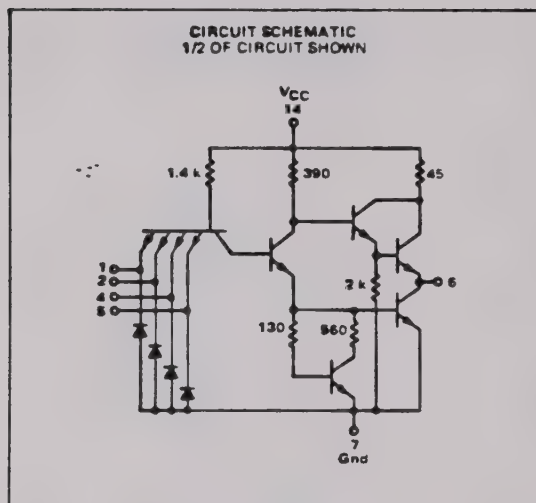
VOLTAGE WAVEFORMS AND DEFINITIONS



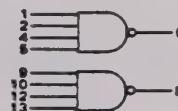
TTL DUAL 4-INPUT NAND BUFFER GATE

MC3024P

665-00146



This device consists of two 4-input NAND power gate circuits. Each gate is designed for driving high fan-out loads (30).



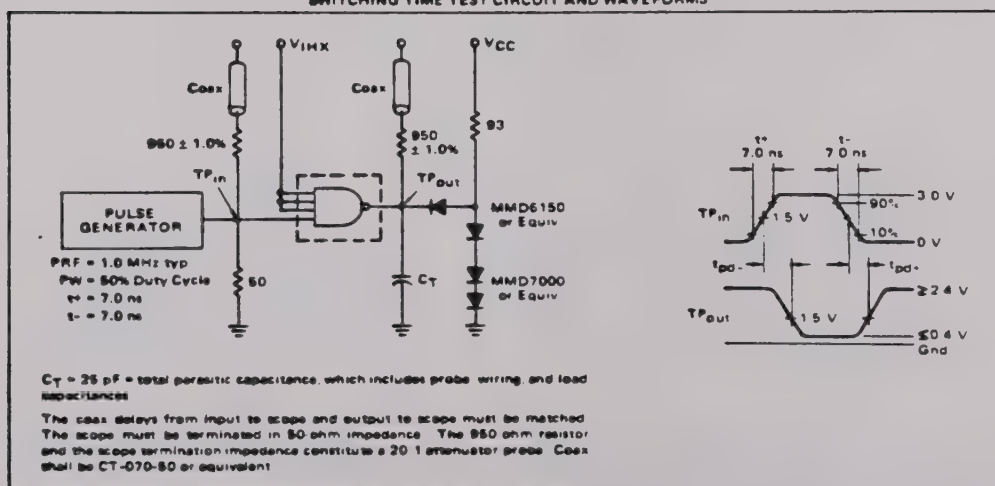
Positive Logic $6 = 1 + 2 + 4 + 5$
Negative Logic $6 = 1 + 2 + 4 + 5$

Input Loading Factor = 2
Output Loading Factor = 30
Total Power Dissipation = 80 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

Pin numbers for the 54H40F/74H40F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3124F, L/3024F, LP	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H40F/74H40F	1	12	3	13	14	2	11	10	6	7	5	8	9	4

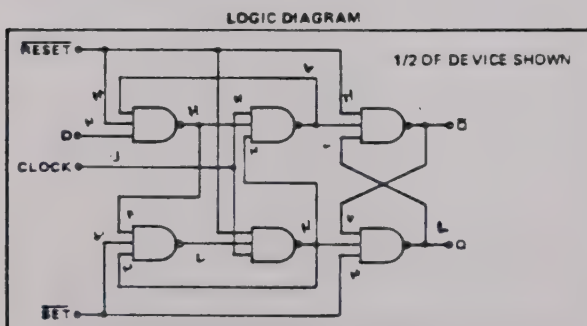
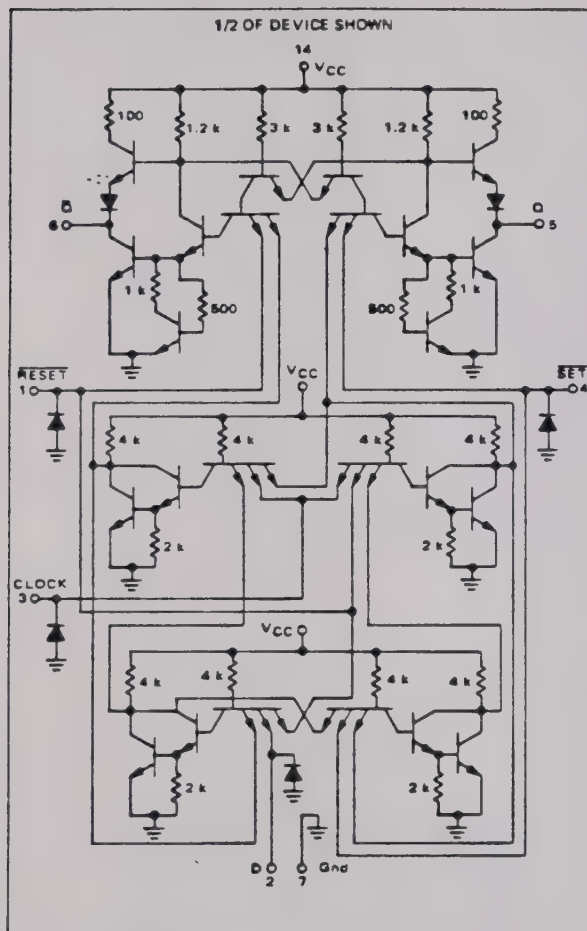
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TTL DUAL D POS EDGE-TRIG FLIP-FLOP W/PRST & CLEAR

MC3060P

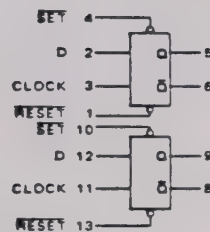
665-00056



This dual flip-flop triggers on the positive edge of the clock and performs the Type D flip-flop logic function. This device consists of two completely independent Type D flip-flops, both having direct SET and RESET inputs for asynchronous operations such as parallel data entry in shift register applications.

Information may be applied to, or changed at the D inputs any time during the clock cycle except during the time interval between the Setup and Hold times. The clocked inputs are inhibited when the clock is high and data may be applied to the input steering section of the flip-flop when the clock goes low. The input steering section continually reflects the input state being applied when the clock is low. The information present at the inputs during the time interval between the Setup and Hold times is transferred to the bistable section on the positive edge of the clock, and the outputs Q and $\bar{Q}$ respond accordingly.

The flip-flop can also be set or reset directly at any time, regardless of the state of the clock, by applying a low state to the direct SET or RESET inputs.



TRUTH TABLE

D	Q^n	Q^{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$$Q^{n+1} = D^n$$

Input Loading Factors

SET = 1.15

RESET = 1.7

CLOCK = 1.5

D = 0.75

Output Loading Factor = 10

Typical Characteristics ($V_{CC} = 5.0V$, $T_A = 25^\circ C$)

Total Power Dissipation = 120 mW/pkg

Toggle Frequency = 30 MHz

Logical "1" Setup Time = 10 ns

Logical "0" Setup Time = 5.0 ns

Logical "1" and "0" Hold Times = 5.0 ns

 $t_{pd} = 17$ ns $t_{pd} = 18$ ns

TTL DUAL D POS EDGE-TRIG FLIP-FLOP W/PRST & CLEAR

(cont'd)

MC3060P

665-00056

OPERATING CHARACTERISTICS

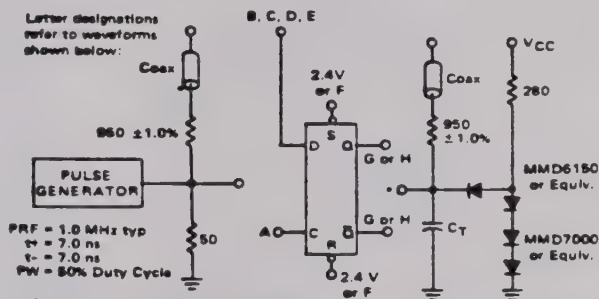
Data must be present 15 ns prior to the rise of the clock and remain 5.0 ns after the clock signal rises.

The direct **SET** and **RESET** inputs may be used at any time as they completely override the clock.

Positive edge triggering When the clock goes from the low to the high state, the information in the input steering section is transferred to the bistable section.

Unused inputs should be tied to a voltage between 2.0 and 5.5 Vdc.

SWITCHING TIME TEST CIRCUIT



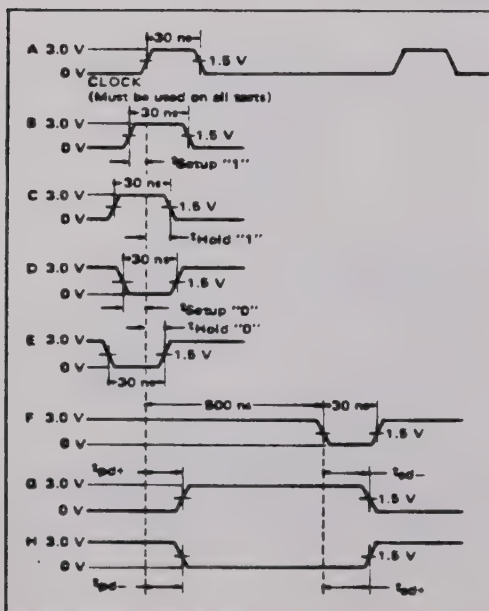
Three pulse generators are required and must be slaved together to provide the waveforms shown.

* A load is connected to each output during the test.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST	INPUT			Q*	Q̄*	LIMITS (ns)		
	D*	SET*	RESET*			Min	Max	
Setup "1" D	B	2.4 v	F	G	H	-	15	
Setup "1" D	C	2.4 v	F	G	H	-	5.0	
Setup "0" D	D	F	2.4 v	H	G	-	15	
Setup "0" D	E	F	2.4 v	H	G	-	5.0	
t _{pd} +	Data from clock to Q during Setup "1" D test						10	25
	Data from clock to Q during Setup "0" D test							
t _{pd} -	Data from clock to Q during Setup "0" D test						10	25
	Data from clock to Q during Setup "1" D test							
t _{pd} +	Data from SET to Q during Setup "0" D test						5.0	20
	Data from RESET to Q during Setup "1" D test							
t _{pd} -	Data from SET to Q during Setup "0" D test						5.5	20
	Data from RESET to Q during Setup "1" D test							

* Letters shown in these columns refer to waveforms on left.

TTL DUAL J-K MASTER-SLAVE FLIP-FLOP WITH CLEAR

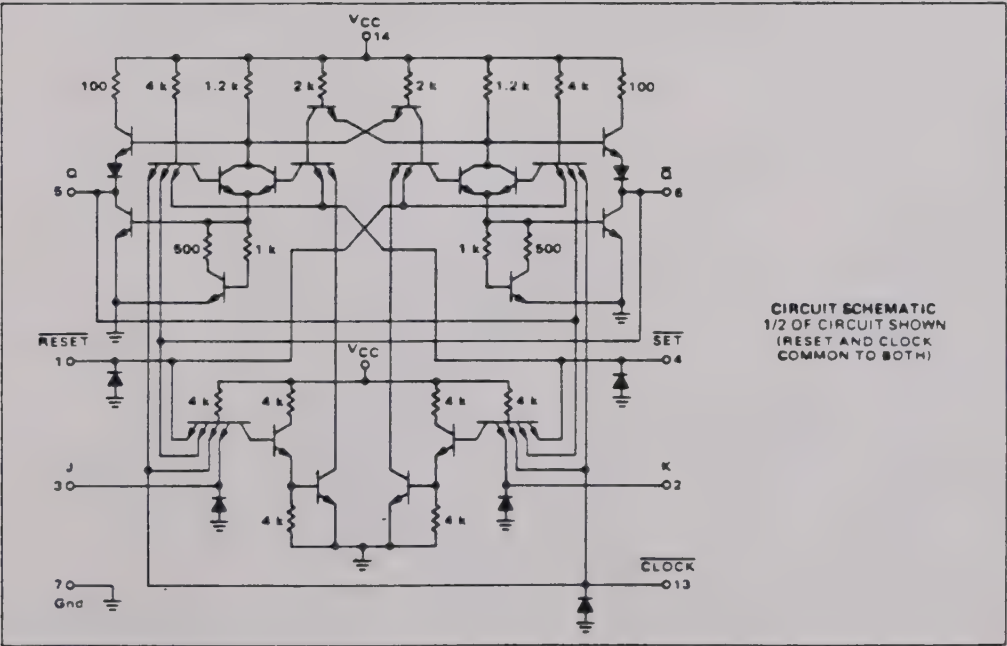
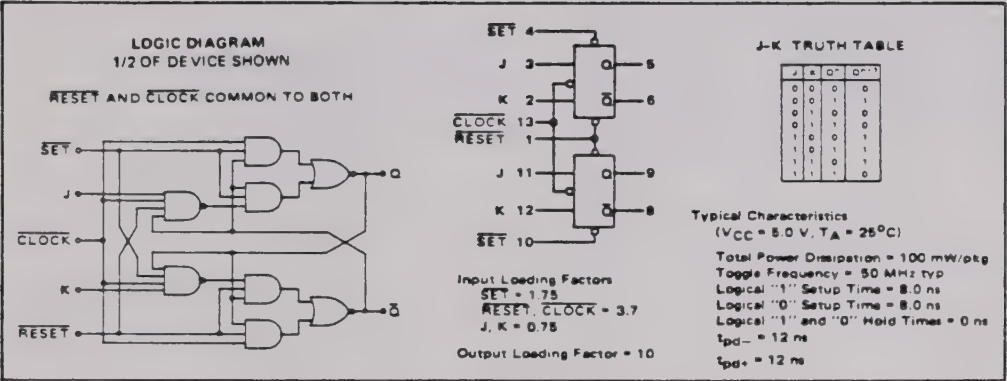
MC3061P

665-00054

This dual JK flip-flop triggers on the negative edge of clock. Each flip-flop is provided with a separate direct SET input in addition to the common direct RESET input. These direct inputs provide a means of resetting a group of flip-flops such as a register which may be followed by the presetting of a data pattern. The clock input for this device is common for both flip-flops, making it particularly useful in registers or other common clock applications.

Data may be applied to or changed at the clocked inputs at any time during the clock cycle, except during the time interval between

the Setup and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between the Setup and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at any time without regard to the clock state by applying a low level to the SET input. In addition, both flip-flops may be reset simultaneously by using the common RESET in a similar manner.



CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN
(RESET AND CLOCK
COMMON TO BOTH)

TTL DUAL J-K MASTER-SLAVE FLIP-FLOP WITH CLEAR
(cont'd)

MC3061P

665-00054

OPERATING CHARACTERISTICS

High state data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

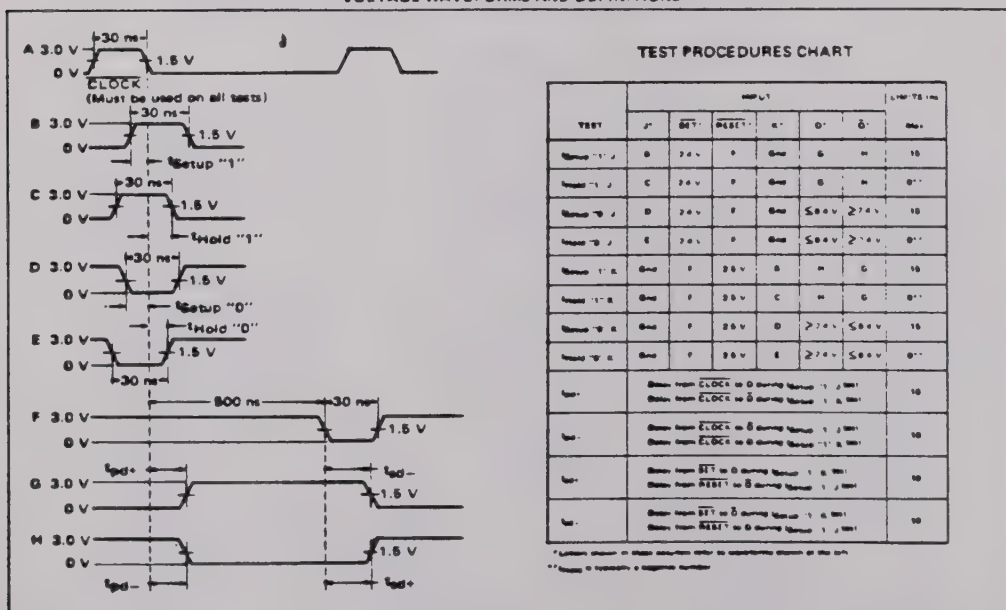
The direct SET (individual) inputs and RESET (common) inputs may be used at any time without regard to the clock state. The flip-flop is set to the $Q = 1$ state by applying a low level to the SET input or reset to the $Q = 0$ state by applying a low level to the RESET input. If these inputs are not used they should be returned to a vol-

ages between 2.0 and 5.5 Vdc.

Negative edge triggering – The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low. The clock fall time must be less than 50 ns.

Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.

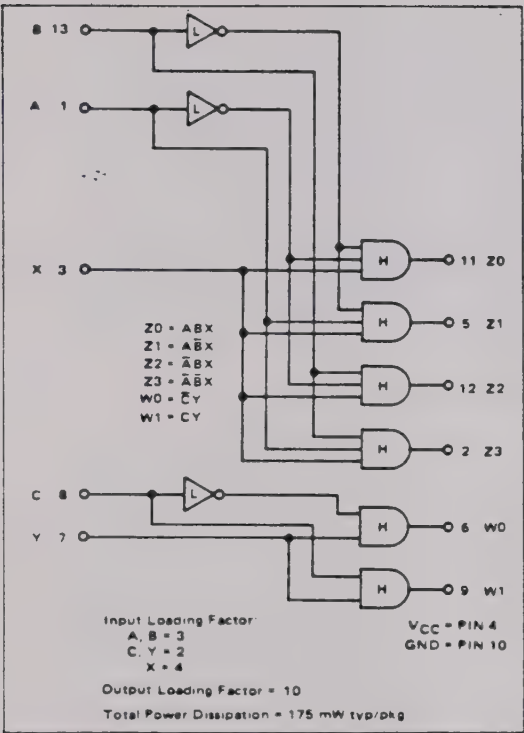
VOLTAGE WAVEFORMS AND DEFINITIONS



TTL 32x8 STATIC RAM

MC4002P

665-00151



ADVANCE INFORMATION/NEW PRODUCT

This device consists of two data distributors constructed from high-level AND gates and low-level inverters. One distributes information present at the input line to one of four output lines; the other distributes information present at the input to one of two output lines. The routing path is selected by the logic signals at the control lines A, B or C.

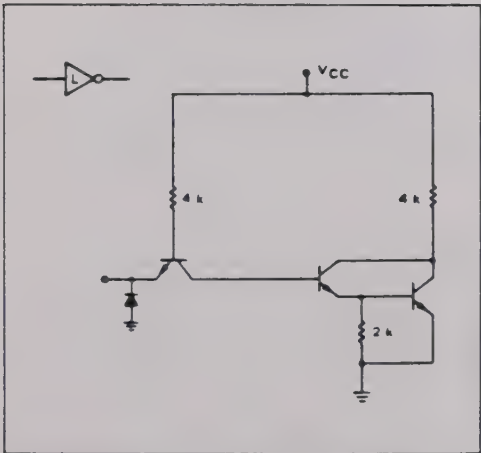
Data distributors are useful in applications where digital data is to be routed from a single register or location to one of several registers or locations for processing.

TYPICAL PROPAGATION DELAY TIMES (ns)
T_A = 25°C

INPUT	Z0	Z1	Z2	Z3
A	14.5	10.5	14.5	10.5
B	14.5	14.5	10.5	10.5
X	10.5	10.5	10.5	10.5

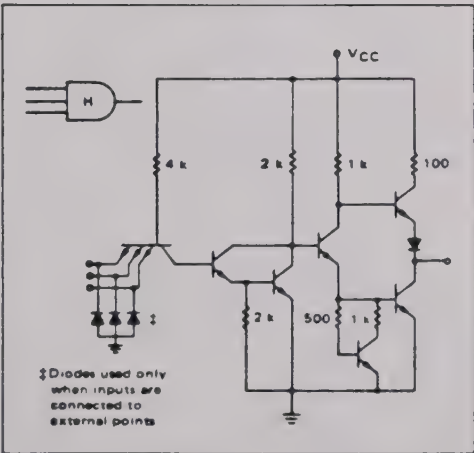
INPUT	W0	W1
C	14.5	10.5
Y	10.5	10.5

LOW-LEVEL INVERTER



*F suffix = TO-86 ceramic flat package (Case 607)
L suffix = TO-116 ceramic dual in-line package (Case 632)
P suffix = TO-116 plastic dual in-line package (Case 606)

HIGH-LEVEL "AND" GATE

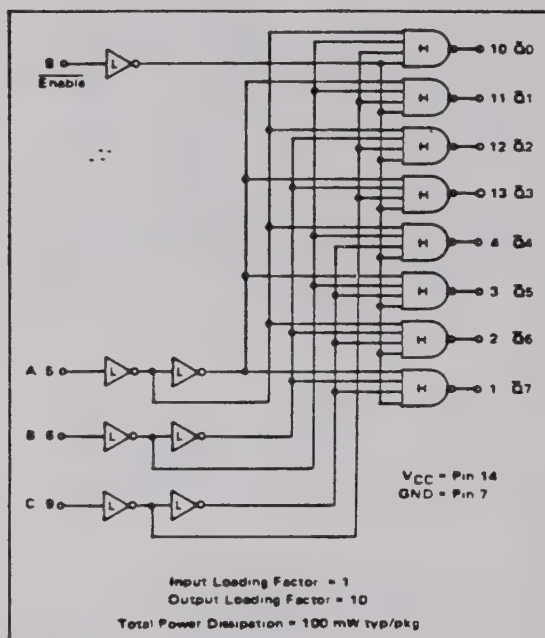


‡Diodes used only when inputs are connected to external points

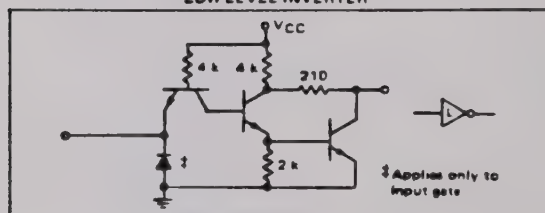
TTL BINARY TO OCTAL (1 OF 8) DECODER

MC4006P

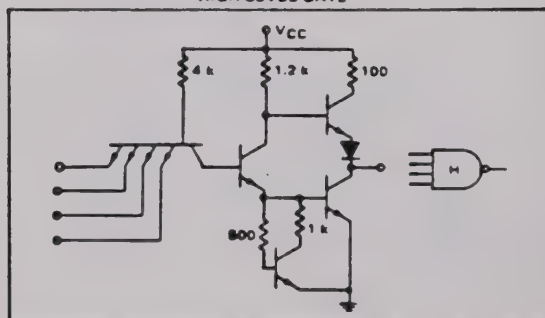
665-00057



LOW-LEVEL INVERTER



HIGH-LEVEL GATE



*F suffix = TO-86 ceramic flat package (Case 807)
L suffix = TO-118 dual in-line ceramic package (Case 832)
P suffix = TO-118 dual in-line plastic package (Case 806).

This device converts three lines of input data to a one-of-eight output. The enable line provides an inhibit capability and also allows the decoder to be expanded for larger decoder systems.

The 3-input/8-output decoder consists of high-level and low-level gates internally connected for minimum power consumption and maximum driving capabilities. The enable gate must be in the low state to perform the decode operation shown in the truth table.

The propagation delays shown in the charts are typical and vary according to loading, interconnection wiring length, and the number of logic levels involved.

E = 0 TRUTH TABLE

C	B	A	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	0	1
0	1	0	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	1	1	0	1	1	1	1
1	0	1	1	1	0	1	1	1	1	1
1	1	0	1	0	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1

1 = High State
0 = Low State

TYPICAL TURN-ON DELAY TIMES (ns)
T_A = 25°C C_T = 20 pF

INPUT	D0	D1	D2	D3	D4	D5	D6	D7
A	11.5	16.0	11.5	16.0	11.5	16.0	11.5	16.0
B	11.0	11.5	16.0	16.0	11.5	11.5	16.0	16.0
C	11.5	11.5	11.5	11.5	16.0	16.0	16.0	16.0
E	12.5	12.5	12.5	12.5	12.5	12.5	12.5	12.5

TYPICAL TURN-OFF DELAY TIMES (ns)
T_A = 25°C C_T = 20 pF

INPUT	D0	D1	D2	D3	D4	D5	D6	D7
A	14.0	19.5	14.0	19.5	14.0	19.5	14.0	19.5
B	14.0	14.0	19.5	19.5	14.0	14.0	19.5	19.5
C	14.0	14.0	14.0	14.0	19.5	19.5	19.5	19.5
E	16.5	16.5	16.5	16.5	16.5	16.5	16.5	16.5

TTL BINARY TO OCTAL (1 OF 8) DECODER (cont'd)

MC4006P

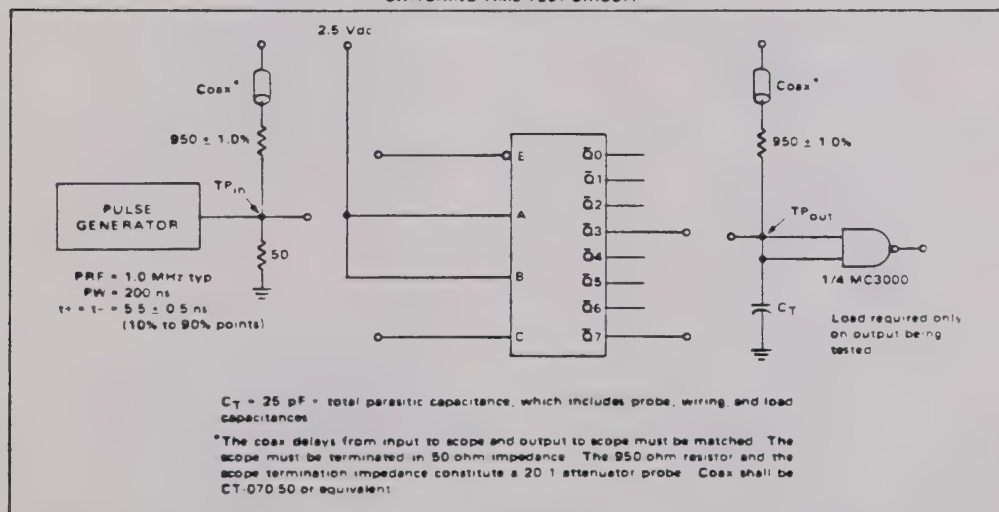
665-00057

INPUT AND OUTPUT LOADING FACTORS with respect to MTTL and MDTL families

FAMILY	MC4006 INPUT LOADING FACTOR	MC4006 OUTPUT LOADING FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.8	8
MC7400	1.0	10
MC830	1.15*	12

*Applies only when input is being driven by MDTL gate with 2.0 kilohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 kilohm pullup resistors reduce drive capability to fan-out of 3.

SWITCHING TIME TEST CIRCUIT

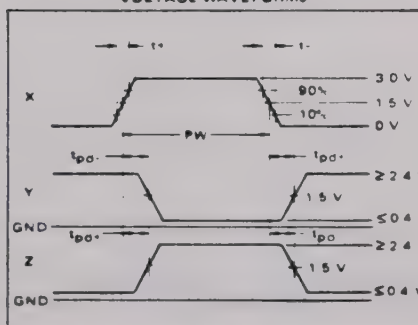


SWITCHING TIME TEST PROCEDURES ($T_A = 25^\circ\text{C}$)

(Letters shown in test columns refer to waveforms)

TEST	E	C	$\bar{O}3$	$\bar{O}7$	LIMITS	
					Max	Unit
t_{pd} (C to $\bar{O}3$)	Gnd	X	Z	-	20	ns
t_{pd} (C to $\bar{O}7$)	Gnd	X	Z	-	17	ns
t_{pd} (C to $\bar{O}3$)	Gnd	X	-	Y	29	ns
t_{pd} (C to $\bar{O}7$)	Gnd	X	-	Y	23	ns
t_{pd} ($\bar{E}$ to $\bar{O}3$)	X	2.5 V	-	Z	21	ns
t_{pd} ($\bar{E}$ to $\bar{O}7$)	X	2.5 V	-	Z	20	ns

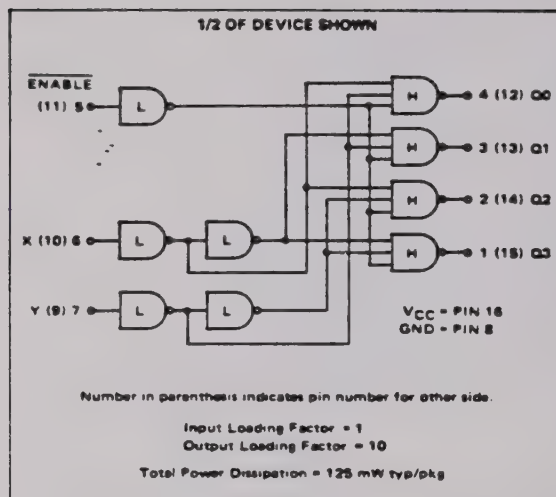
VOLTAGE WAVEFORMS



TTL DUAL BINARY 1-OF-4 LINE GATED DECODER

MC4007P

665-00149



This device converts two lines of input data to a one-of-four output. The enable line provides an inhibit capability and also allows the decoder to be expanded for larger decoder systems.

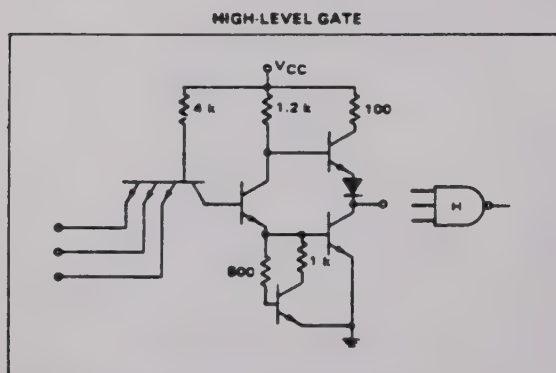
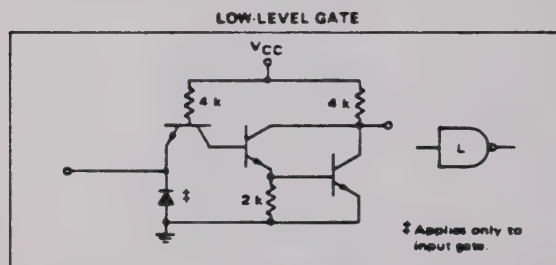
The dual 2-input/4-output decoder consists of high-level and low-level gates internally connected for minimum power consumption and maximum driving capabilities. The enable gate must be in the low state to perform the decode operation shown in the truth table.

The propagation delays shown in the charts are typical and vary according to loading, interconnection wiring length, and the number of logic levels involved.

E = 0 TRUTH TABLE

X	Y	Q0	Q1	Q2	Q3
0	0	0	1	1	1
1	0	1	0	1	1
0	1	1	1	0	1
1	1	1	1	1	0

1 = High State
 0 = Low State



L suffix = 16-pin dual in-line ceramic package (Case 620).
 P suffix = 16-pin in-line plastic package (Case 612).

TYPICAL TURN-ON DELAY TIMES (ns)
T_A = 25°C

Input	Q0	Q1	Q2	Q3
X	11.5	15.5	11.5	15.5
Y	11.5	11.5	15.5	15.5
E	13.5	13.5	13.5	13.5

TYPICAL TURN-OFF DELAY TIMES (ns)
T_A = 25°C

Input	Q0	Q1	Q2	Q3
X	14.0	19.0	14.0	19.0
Y	14.0	14.0	19.0	19.0
E	14.5	14.5	14.5	14.5

TTL DUAL BINARY 1-OF-4 LINE GATED DECODER
(cont'd)

MC4007P

665-00149

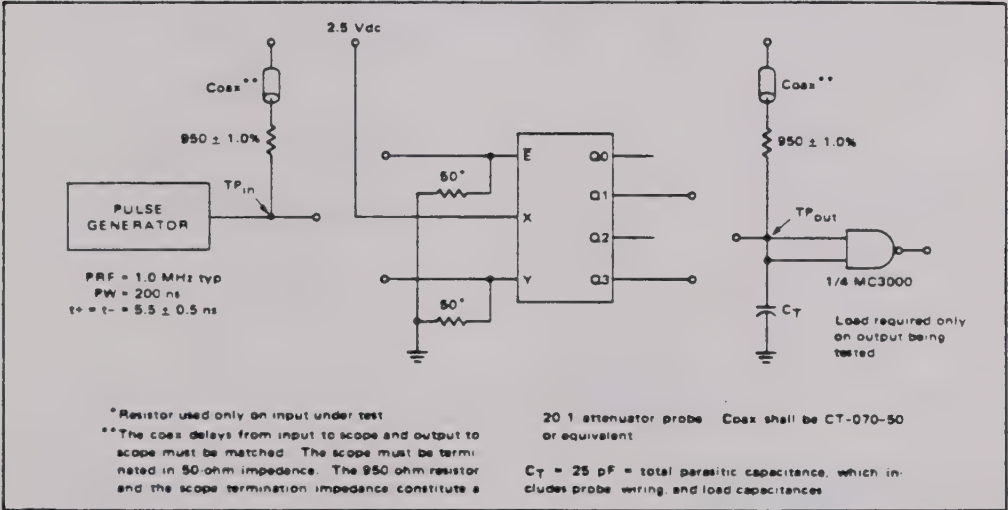
INPUT LOADING and OUTPUT DRIVING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT DRIVE FACTOR
MC4000	1.0	10
MC600	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	10
MC830	1.15**	12

Note: Differences in MC4000 series loading factors result from differences in specifications for each family

** Applies only when input is being driven by MDTL gate with 2 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6 k ohm pullup resistors reduce drive capability to fan-out of 3.

SWITCHING TIME TEST CIRCUIT

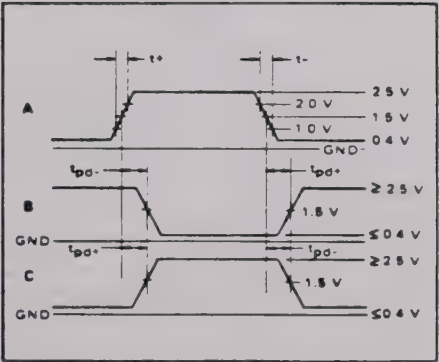


TEST PROCEDURES

(Letters shown in test columns refer to waveforms)

TEST	E	Y	Q1	Q3	LIMITS	
					Max	Unit
t _{pd+} (Y to Q1)	Gnd	A	C	-	20	ns
t _{pd-} (Y to Q1)	Gnd	A	C	-	17	ns
t _{pd+} (Y to Q3)	Gnd	A	-	B	29	ns
t _{pd-} (Y to Q3)	Gnd	A	-	B	23	ns
t _{pd+} (E to Q3)	A	2.5 V	-	C	21	ns
t _{pd-} (E to Q3)	A	2.5 V	-	C	20	ns

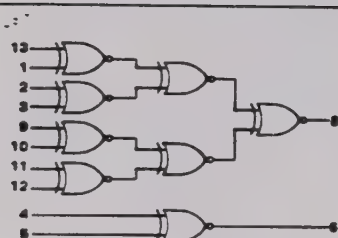
VOLTAGE WAVEFORMS



TTL 8-BIT PARITY TREE

MC4008P

665-00150



V_{CC} = Pin 14
GND = Pin 7

Positive Logic:

8 = 1 ⊕ 2 ⊕ 3 ⊕ 4 ⊕ 10 ⊕ 11 ⊕ 12 ⊕ 13

5 = 4 ⊕ 5

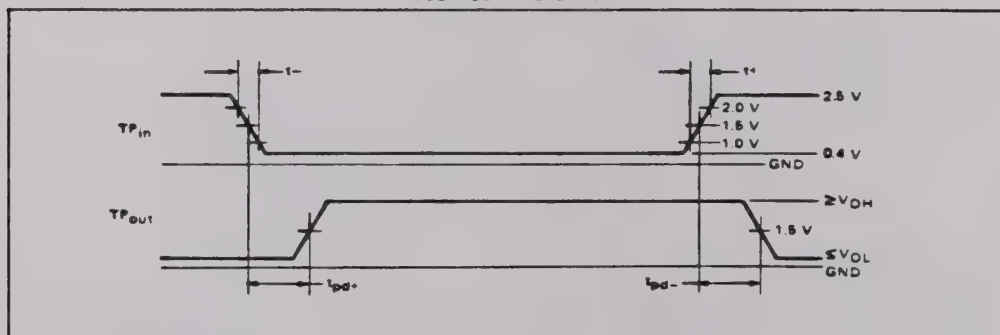
where $X \oplus Y = (\bar{X} \cdot \bar{Y}) + (X \cdot Y)$

This device consists of seven Exclusive NOR gates connected to check even parity. The output will be in the logic "1" state as long as the "1" state is present on an even number of inputs. The additional Exclusive NOR gate can be used to connect two 8-bit parity trees to form a 16-bit parity tree, or it can be used to convert the parity tree to check odd parity by connecting one gate input to the output of the parity tree and grounding the other input. This conversion can also be accomplished by connecting a simple inverter to the output of the parity tree.

Input Loading Factor = 2
Output Loading Factor = 10

Total Power Dissipation = 150 mW typ/pkg
Propagation Delay Time = 15-30 ns typ

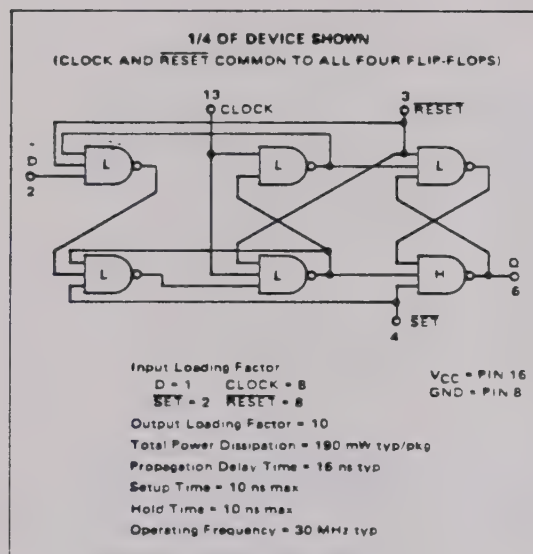
VOLTAGE WAVEFORMS



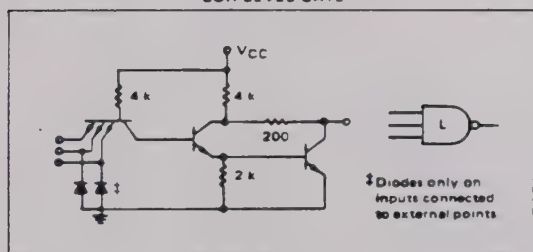
TTL QUAD TYPE D FLIP-FLOP

MC4015P

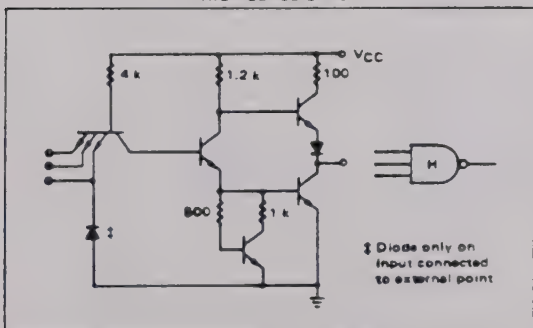
665-00144



LOW-LEVEL GATE



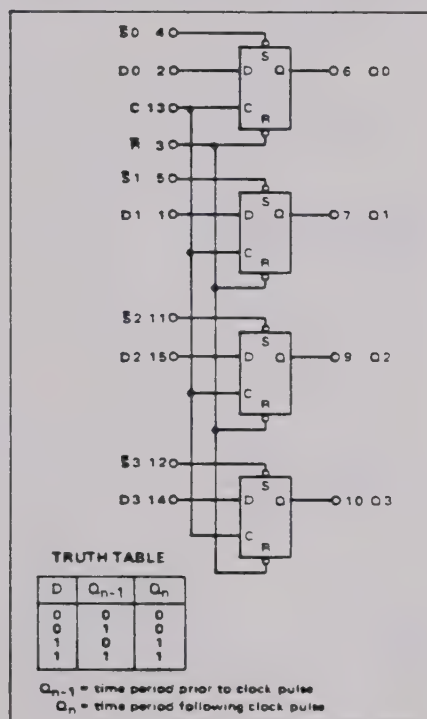
HIGH-LEVEL GATE



- * L suffix = 16-pin dual in-line ceramic package (Case 620)
P suffix = 16-pin dual in-line plastic package (Case 612)

This quad type D flip-flop triggers on the positive edge of the clock input. During the clock transition the state of the D input is transferred to the Q output. The device is useful in shift registers and simple counters.

Power dissipation is minimized and output drive capability is maximized by connecting low and high-level gates as shown by the logic diagram to form each of the four flip-flops.



OPERATING CHARACTERISTICS

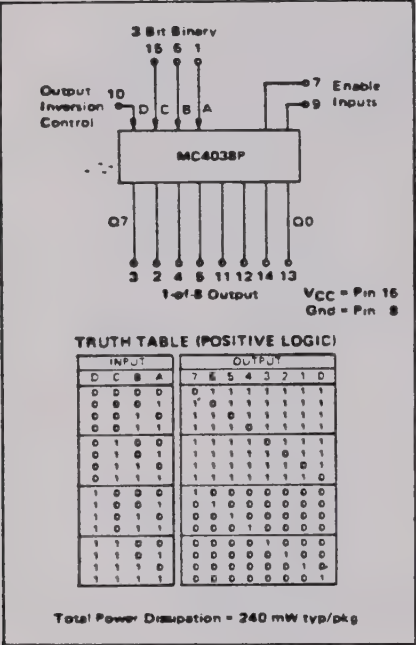
Data must be present at the D input 10 ns prior to the rise of the clock, and remain 10 ns after the clock signal rises. Data may be changed any time during the clock cycle except the interval between the setup time (10 ns) and the hold time (10 ns) without affecting the operation of the flip-flop. The data input is inhibited when the clock is high. When the clock is in the low state, the input steering section continually reflects the state of the D input. Information present at the D input during the time interval between the setup and hold times is transferred to the bistable section on the positive edge of the clock, and outputs Q and $\bar{Q}$ respond accordingly.

The flip-flops can be set or reset directly at any time, regardless of the state of the clock, by applying a low state to the direct Set or Reset inputs.

TTL INVERTING/NON-INVERTING ONE-OF-EIGHT DECODER

MC4038P

665-00123

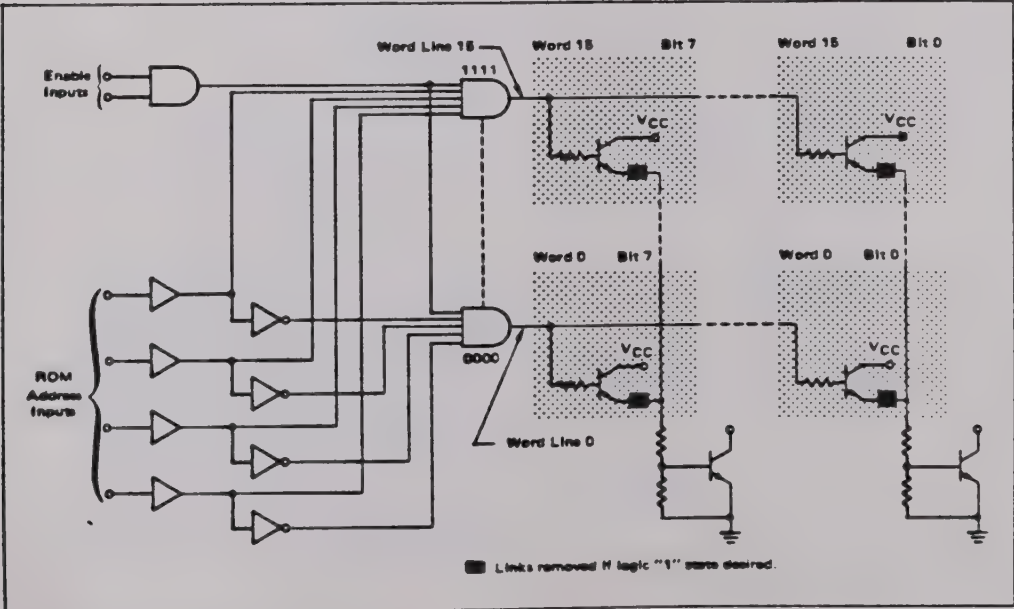


The MC4038P is derived from the XC170 128-Bit Read Only Memory. A 3-bit binary address selects the desired word for the 8-bit output. The inversion control, D, selects half of the memory chip with the bit pattern that defines a 1-of-8 decoder function. When D is a logic "0", the selected output is designated as a logic "0". A logic "1" on D produces a logic "1" on the selected output.

- Features:
- Address times < 45 ns
 - Outputs sink 20 mA
 - Output capacitance < 7.0 pF @ 1.5 V
 - Wired OR capability to 64 memories

ENABLE INPUT TRUTH TABLE (POSITIVE LOGIC)

E	E	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	FUNCTION ENABLED							

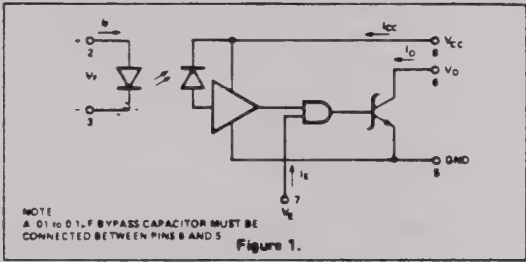


*P suffix = 16-pin dual in-line plastic package (Case 612).

DTL/TTL COMPATIBLE OPTICALLY COUPLED GATE

6N137(5082-4360)

665-00210



Features

- DTL/TTL COMPATIBLE: 5V SUPPLY
- ULTRA HIGH SPEED
- LOW INPUT CURRENT REQUIRED
- HIGH COMMON MODE REJECTION
- GUARANTEED PERFORMANCE OVER TEMPERATURE
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)
- 3000V dc INSULATION VOLTAGE

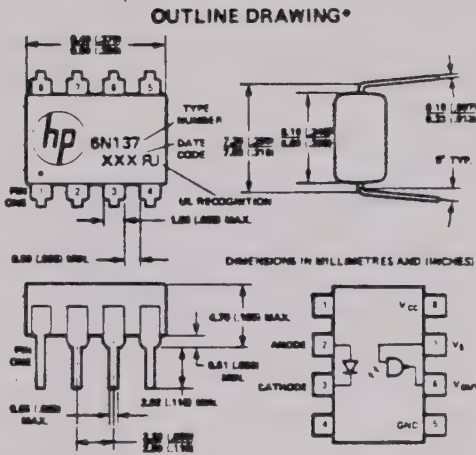
Description/Applications

The 6N137 consists of a GaAsP photon emitting diode and a unique integrated detector. The photons are collected in the detector by a photodiode and then amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. The circuit is temperature, current and voltage compensated.

This unique isolator design provides maximum DC and AC circuit isolation between input and output while achieving DTL/TTL circuit compatibility. The isolator operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5mA will sink an eight gate fan-out (13mA) at the output with 5 volt Vcc applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 45nsec. The enable input provides gating of the detector with input sinking and sourcing requirements compatible with DTL/TTL interfacing and a propagation delay of 25 ns typical.

The 6N137 can be used in high speed digital interfacing applications where common mode signals must be rejected, such as for a line receiver and digital programming of floating power supplies, motors, and other machine control systems. The elimination of ground loops can be accomplished in system interfaces such as between a computer and a peripheral memory, printer, controller, etc.

The open collector output provides capability for bussing, OR'ing and strobing.



Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	IFL	0	250	µA
Input Current, High Level Each Channel	IFH	6.3**	10	mA
High Level Enable Voltage	VEH	2.0	5.5	V
Low Level Enable Voltage (Output High)	VEL	0	0.8	V
Supply Voltage, Output	VCC	4.5	5.5	V
Fan Out (TTL Load)	N		8	
Operating Temperature	TA	0	70	°C

Absolute Maximum Ratings*

(No derating required up to 70°C)

Storage Temperature	-55°C to +125°C
Operating Temperature	0°C to +70°C
Lead Solder Temperature	260°C for 10s (1.6mm below seating plane)
Peak Forward Input Current	20mA (≤ 1 msec Duration)
Average Forward Input Current	10mA
Reverse Input Voltage	5V
Enable Input Voltage	5.5V (Not to exceed Vcc by more than 500mV)
Supply Voltage - Vcc	7V (1 Minute Maximum)
Output Current - Io	50mA
Output Collector Power Dissipation	85mW
Output Voltage - Vo	7V

**6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less

VOLTAGE REGULATOR

LM723

665-00164

Voltage Regulators

LM723/LM723C voltage regulator

general description

The LM723/LM723C is a voltage regulator designed primarily for series regulator applications. By itself, it will supply output currents up to 150 mA, but external transistors can be added to provide any desired load current. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting. Important characteristics are:

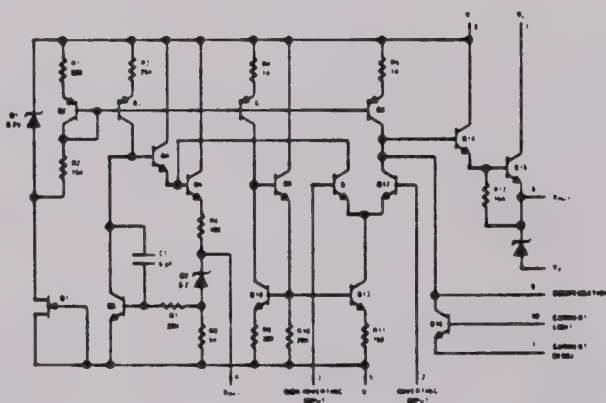
- 150 mA output current without external pass transistor
- Output currents in excess of 10A possible by adding external transistors

- Input voltage 40V max
- Output voltage adjustable from 2V to 37V
- Can be used as either a linear or a switching regulator.

The LM723/LM723C is also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature controller.

The LM723C is identical to the LM723 except that the LM723C has its performance guaranteed over a 0°C to 70°C temperature range, instead of -55°C to +125°C.

schematic and connection diagrams*



Dual-In-Line Package



Order Number LM723D or LM723CD
See Package 1

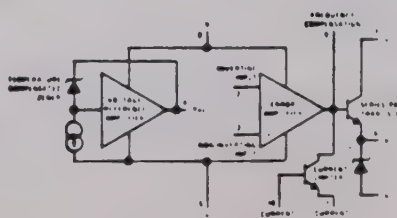
Order Number LM723N or LM723CN
See Package 22

Metal Can Package



Order Number LM723H or LM723CH
See Package 13

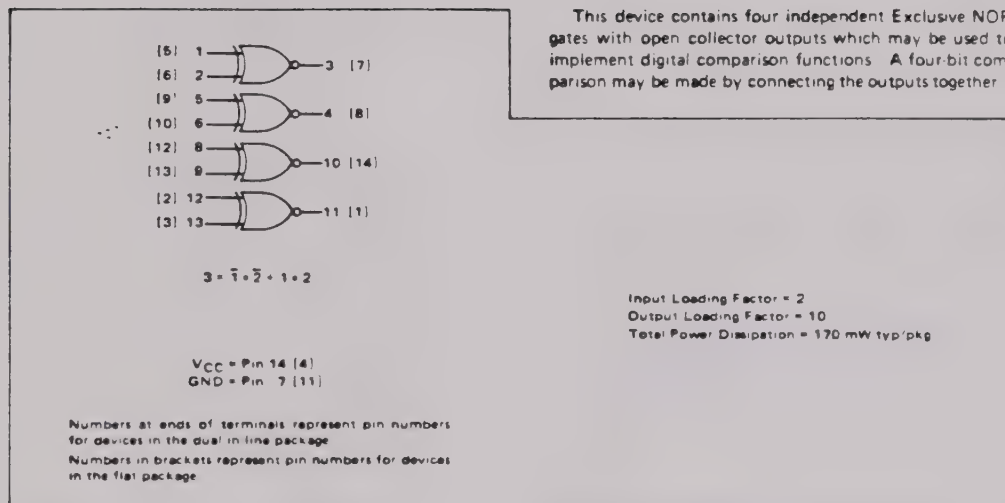
equivalent circuit*



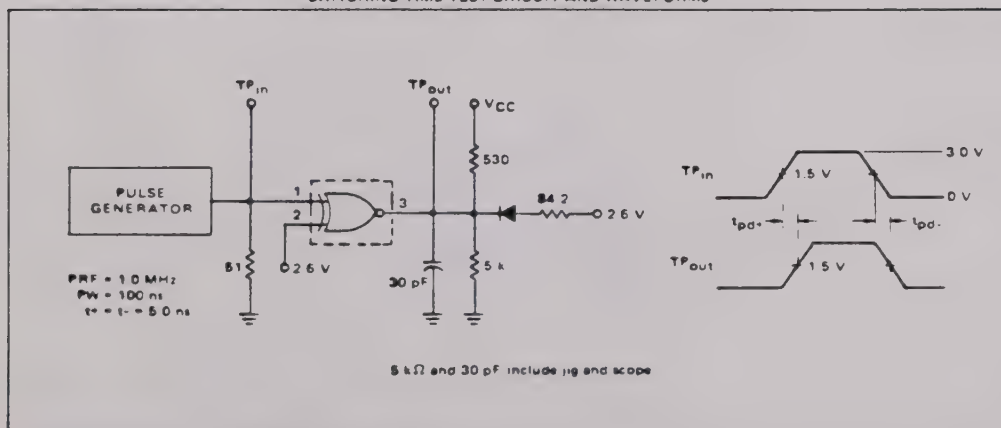
TTL QUAD 2-INPUT EXCLUSIVE NOR GATE

MC7242P

665-00154



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



*F suffix = TO-86 ceramic flat package (Case 607)

*L suffix = TO-116 ceramic dual in-line package (Case 632)

*P suffix = TO-118 plastic dual in-line package (Case 605)

TTL QUAD 2-INPUT 4-BIT MULTIPLEXER

MC7266P or S/N8266

665-00152

DESCRIPTION

The 8266/8267 2-Input, 4-Bit Digital Multiplexer is a monolithic array utilizing familiar TTL circuit structures. The 8267 features a bare-collector output to allow expansion with other devices.

The multiplexer is intended for use at the inputs to adders, registers and in other parallel data handling applications.

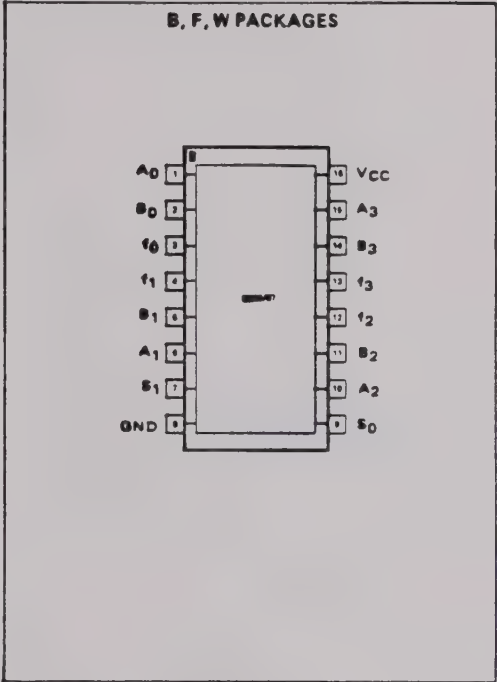
The multiplexer is able to choose from two different input sources, each containing 4 bits: $A = (A_0, A_1, A_2, A_3)$, $B = (B_0, B_1, B_2, B_3)$. The selection is controlled by the input S_0 , while the second control input, S_1 , is held at zero.

For conditional complementing, the two inputs (A_n, B_n) are tied together to form the function TRUE/COMPLEMENT, which is needed in conjunction with added elements to perform ADDITION/SUBTRACTION. Further, the inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

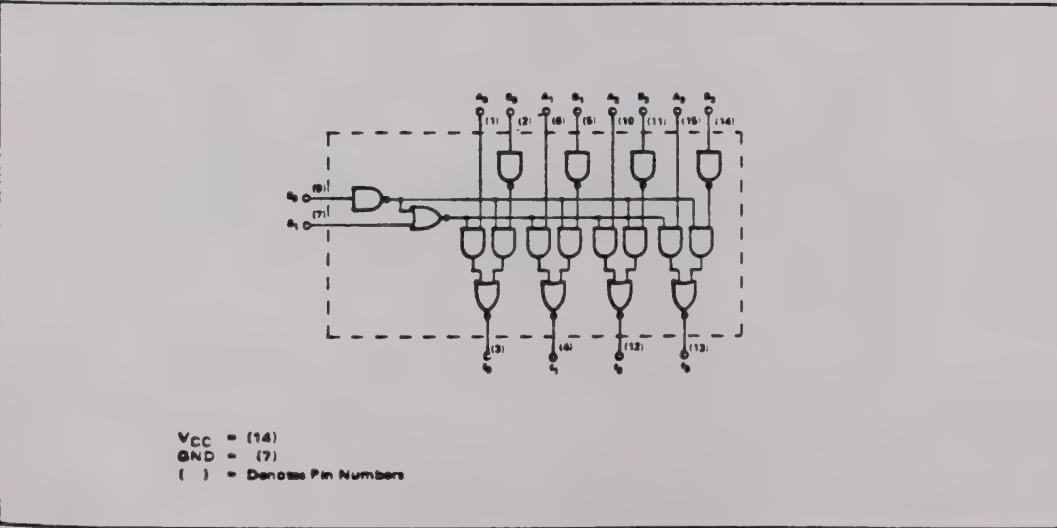
TRUTH TABLE

SELECT LINES		OUTPUTS
S_0	S_1	f_n (0, 1, 2, 3)
0	0	B_n
0	1	$\bar{B}_n$
1	0	A_n
1	1	1

PIN CONFIGURATIONS (Top View)



LOGIC DIAGRAM

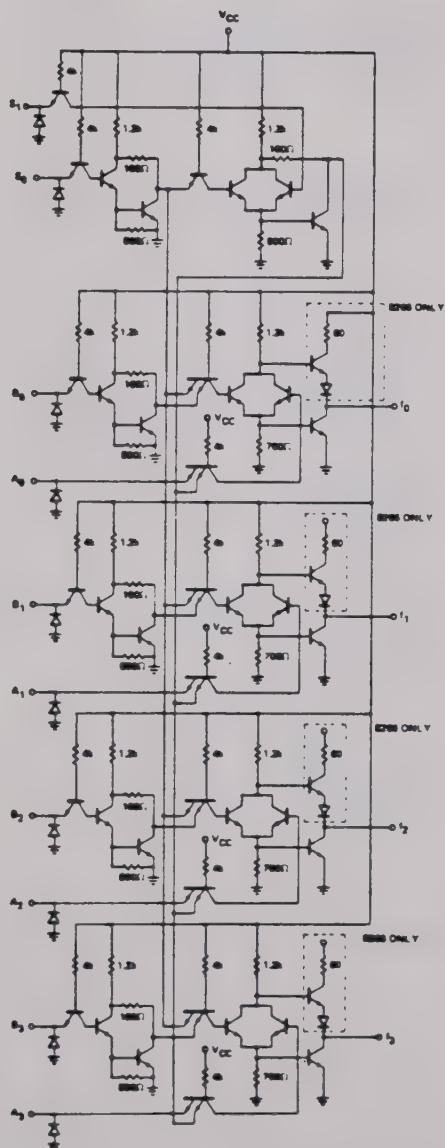


TTL QUAD 2-INPUT 4-BIT MULTIPLEXER
(cont'd)

MC7266P or S/N8266

665-00152

SCHEMATIC DIAGRAM



TTL QUADRUPLE 2-INPUT POSITIVE NAND GATE

SN74LS00

665-00137

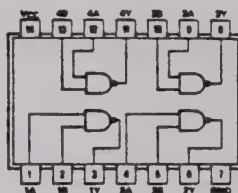
665-00024

QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

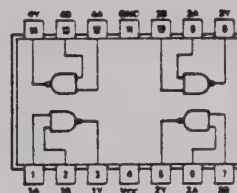
00

positive logic:

$$Y = \overline{AB}$$



SN5400 (J) SN7400 (J, N)
 SN54H00 (J) SN74H00 (J, N)
 SN54L00 (J) SN74L00 (J, N)
 SN54LS00 (J, W) SN74LS00 (J, N)
 SN54S00 (J, W) SN74S00 (J, N)



SN5400 (W)
 SN54H00 (W)
 SN54L00 (T)

SN74LS001

SN74H01

665-00094

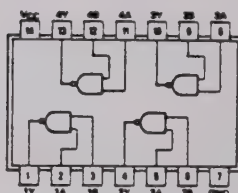
665-00172

QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

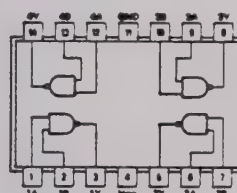
01

positive logic:

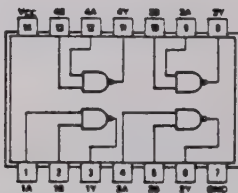
$$Y = \overline{AB}$$



SN5401 (J) SN7401 (J, N)
 SN54LS01 (J, W) SN74LS01 (J, N)



SN5401 (W)
 SN54H01 (W)
 SN54L01 (T)



SN54H01 (J) SN74H01 (J, N)

TTL QUADRUPLE 2-INPUT POSITIVE NOR GATE

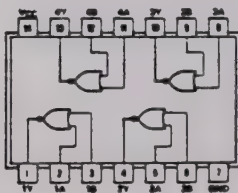
SNL402

QUADRUPLE 2-INPUT
POSITIVE-NOR GATES

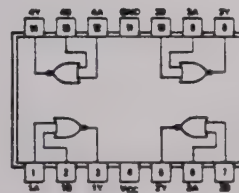
02

positive logic:

$$Y = \overline{A+B}$$



SN5402 (J) SN7402 (J, N)
 SN54L02 (J) SN74L02 (J, N)
 SN54LS02 (J, W) SN74LS02 (J, N)
 SN54S02 (J, W) SN74S02 (J, N)



SN5402 (W)
 SN54L02 (T)

665-00050

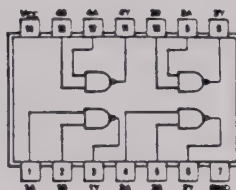
TTL QUADRUPLE 2-INPUT POSITIVE NAND GATE

SN74LS03

QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

03

positive logic:

 $Y = \overline{AB}$ 

NOT USED

SN5403 (J) SN7403 (J, N)
SN54L03 (J) SN74L03 (J, N)
SN54LS03 (J, W) SN74LS03 (J, N)
SN54S03 (J, W) SN74S03 (J, N)

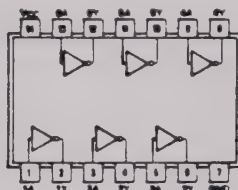
TTL HEX INVERTERS

SN74LS04
SN7404

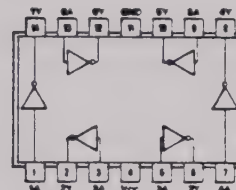
HEX INVERTERS

04

positive logic:

 $Y = \overline{A}$ 

SN5404 (J) SN7404 (J, N)
SN54H04 (J) SN74H04 (J, N)
SN54L04 (J) SN74L04 (J, N)
SN54LS04 (J, W) SN74LS04 (J, N)
SN54S04 (J, W) SN74S04 (J, N)



SN5404 (W)
SN54H04 (W)
SN54L04 (T)

665-00334
665-00085

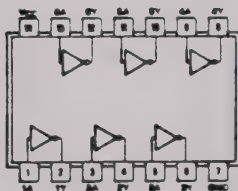
TTL HEX INVERTER

SN74LS05

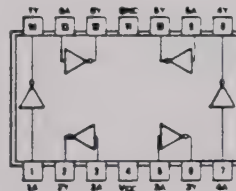
HEX INVERTERS
WITH OPEN-COLLECTOR OUTPUTS

05

positive logic:

 $Y = \overline{A}$ 

SN5405 (J) SN7405 (J, N)
SN54H05 (J) SN74H05 (J, N)
SN54LS05 (J, W) SN74LS05 (J, N)
SN54S05 (J, W) SN74S05 (J, N)



SN5405 (W)
SN54H05 (W)

NOT USED

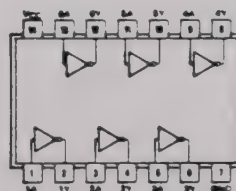
TTL HEX INVERTER BUFFER/DRIVER HIGH VOLTAGE OUTPUT

SN74LS06

HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

06

positive logic:

 $Y = \overline{A}$ 

SN5406 (J, W) SN7406 (J, N)

NOT USED

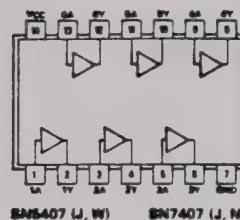
TTL HEX BUFFER DRIVER HIGH-VOLTAGE OUTPUT

SN74LS07

HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

07

positive logic:
Y = A



NOT USED

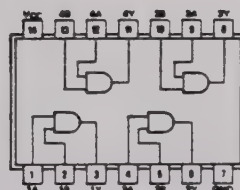
TTL QUADRUPLE 2-INPUT POSITIVE AND GATE

SN74LS08
SN7408

QUADRUPLE 2-INPUT
POSITIVE-AND GATES

08

positive logic:
Y = AB



665-00190

SN7408 (J, W) SN7408 (J, N)
SN74LS08 (J, W) SN74LS08 (J, N)
SN74S08 (J, W) SN74S08 (J, N)

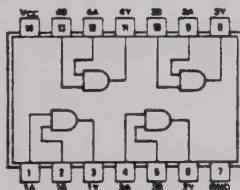
TTL QUADRUPLE 2-INPUT POSITIVE AND GATE

SN74LS09

QUADRUPLE 2-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR OUTPUTS

09

positive logic:
Y = AB



NOT USED

SN7409 (J, W) SN7409 (J, N)
SN74LS09 (J, W) SN74LS09 (J, N)
SN74S09 (J, W) SN74S09 (J, N)

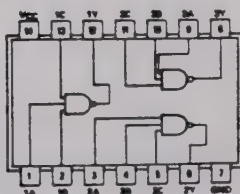
TTL TRIPLE 3-INPUT POSITIVE NAND GATE

SN74LS10
SN7410P

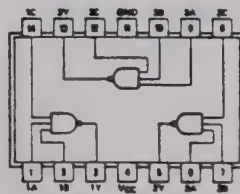
TRIPLE 3-INPUT
POSITIVE-NAND GATES

10

positive logic:
Y = $\overline{ABC}$



SN7410 (J) SN7410 (J, N)
SN74M10 (J) SN74M10 (J, N)
SN74L10 (J) SN74L10 (J, N)
SN74LS10 (J, W) SN74LS10 (J, N)
SN74S10 (J, W) SN74S10 (J, N)



SN7410 (W)
SN74M10 (W)
SN74L10 (T)

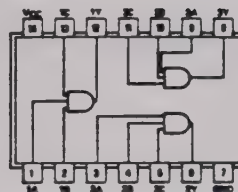
665-00025

TTL TRIPLE 3-INPUT POSITIVE AND GATE

SN74LS15
SN7415

TRIPLE 3-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR OUTPUTS
15

positive logic:
 $Y = ABC$



NOT USED

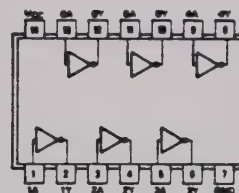
SN54H15 (J, W) SN74H15 (J, N)
SN54LS15 (J, W) SN74LS15 (J, N)
SN54S15 (J, W) SN74S15 (J, N)

TTL HEX INVERTER BUFFER/DRIVER

SN74LS16
SN7416

HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS
16

positive logic:
 $Y = \bar{A}$



NOT USED

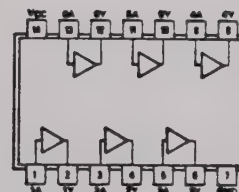
SN5416 (J, W) SN7416 (J, N)

TTL HEX BUFFER/DRIVER

SN74LS17
SN7417

HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS
17

positive logic:
 $Y = A$



NOT USED

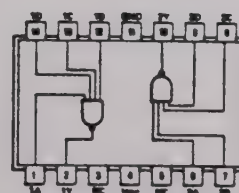
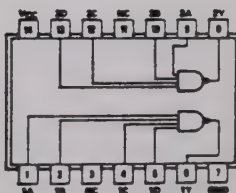
SN5417 (J, W) SN7417 (J, N)

TTL DUAL 4-INPUT POSITIVE NAND GATE

SN74LS20
SN7420

DUAL 4-INPUT
POSITIVE-NAND GATES
20

positive logic:
 $Y = \overline{ABCD}$



665-00088

SN5420 (J) SN7420 (J, N)
SN54H20 (J) SN74H20 (J, N)
SN54L20 (J) SN74L20 (J, N)
SN54LS20 (J, W) SN74LS20 (J, N)
SN54S20 (J, W) SN74S20 (J, N)

SN5420 (W)
SN54H20 (W)
SN54L20 (T)

NC—No internal connection

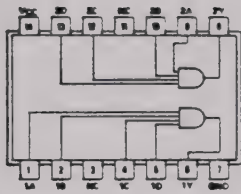
TTL DUAL 4-INPUT POSITIVE AND GATE

SN74LS21
SN7421

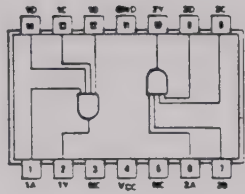
DUAL 4-INPUT
POSITIVE-AND GATES

21

positive logic:
Y = ABCD



SN54H21 (J) SN74H21 (J, N)
SN54LS21 (J, W) SN74LS21 (J, N)



SN54H21 (W)
NC—No internal connection

NOT USED

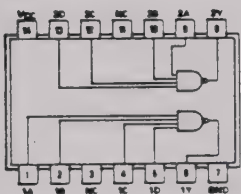
TTL DUAL 4-INPUT POSITIVE NAND GATE

SN74LS22
SN7422

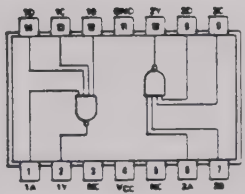
DUAL 4-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

22

positive logic:
Y = ABCD



SN54H22 (J, W) SN7422 (J, N)
SN54H22 (J) SN74H22 (J, N)
SN54LS22 (J, W) SN74LS22 (J, N)
SN54S22 (J, W) SN74S22 (J, N)



SN54H22 (W)
NC—No internal connection

NOT USED

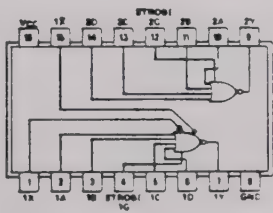
TTL EXPANDABLE DUAL 4-INPUT POSITIVE NOR GATE WITH STROBE

SN74LS23
SN7423

EXPANDABLE DUAL 4-INPUT
POSITIVE-NOR GATES
WITH STROBE

23

positive logic:
 $1Y = 1G(1A+1B+1C+1D)+X$
 $2Y = 2G(2A+2B+2C+2D)$
X = output of SN5460/SN7460



SN5423 (J, W) SN7423 (J, N)

NOT USED

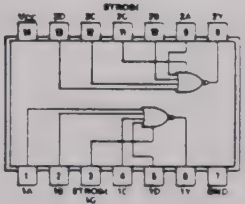
TTL DUAL 4-INPUT POSITIVE NOR GATE WITH STROBE

SN74LS25
SN7425

DUAL 4-INPUT
POSITIVE-NOR GATES
WITH STROBE

25

positive logic:
Y = G(A+B+C+D)



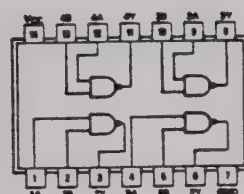
SN5425 (J, W) SN7425 (J, N)

665-00148

TTL QUADRUPLE 2-INPUT POSITIVE NAND GATE

SN74LS26
SN7426QUADRUPLE 2-INPUT
HIGH-VOLTAGE INTERFACE
POSITIVE-NAND GATES

26

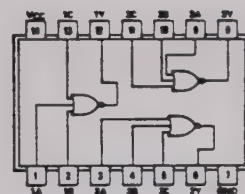
positive logic:
 $Y = \overline{AB}$ SN5426 (J) SN7426 (J, N)
SN54LS26 (J, W) SN74LS26 (J, N)

NOT USED

TTL TRIPLE 3-INPUT POSITIVE NOR GATE

SN74LS27
SN7427TRIPLE 3-INPUT
POSITIVE-NOR GATES

27

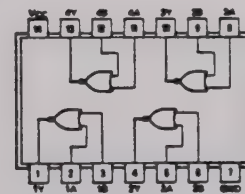
positive logic:
 $Y = \overline{A+B+C}$ SN5427 (J, W) SN7427 (J, N)
SN54LS27 (J, W) SN74LS27 (J, N)

NOT USED

TTL QUADRUPLE 2-INPUT POSITIVE NOR BUFFER

SN74LS28
SN7428QUADRUPLE 2-INPUT
POSITIVE-NOR BUFFERS

28

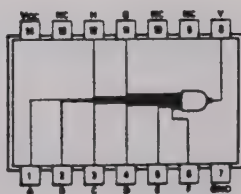
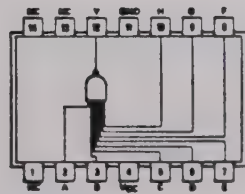
positive logic:
 $Y = \overline{A+B}$ SN5428 (J, W) SN7428 (J, N)
SN54LS28 (J, W) SN74LS28 (J, N)

NOT USED

TTL 8-INPUT POSITIVE NAND GATE

SN74LS30
SN74308-INPUT
POSITIVE-NAND GATES

30

positive logic:
 $Y = \overline{ABCDEFGH}$ SN5430 (J) SN7430 (J, N)
SN54H30 (J) SN74H30 (J, N)
SN54L30 (J) SN74L30 (J, N)
SN54LS30 (J, W) SN74LS30 (J, N)
SN54S30 (J, W) SN74S30 (J, N)SN5430 (W) SN7430 (J, N)
SN54H30 (W) SN74H30 (J, N)
SN54L30 (Y) SN74L30 (J, N)
NC—No internal connection

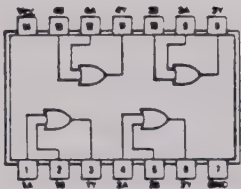
665-00090

TTL QUADRUPL 2-INPUT POSITIVE OR GATE

SN74LS32
SN7432

QUADRUPL 2-INPUT
POSITIVE-OR GATES
32

positive logic:
 $Y = A + B$



NOT USED

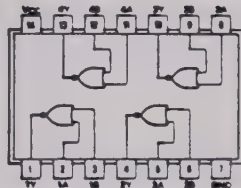
SN5432 (J, W) SN7432 (J, N)
SN54LS32 (J, W) SN74LS32 (J, N)
SN54S32 (J, W) SN74S32 (J, N)

TTL QUADRUPL 2-INPUT POSITIVE NOR BUFFER

SN74LS33
SN7433

QUADRUPL 2-INPUT
POSITIVE-NOR BUFFERS
WITH OPEN-COLLECTOR OUTPUTS
33

positive logic:
 $Y = A + B$



NOT USED

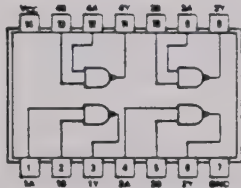
SN5433 (J, W) SN7433 (J, N)
SN54LS33 (J, W) SN74LS33 (J, N)

TTL QUADRUPL 2-INPUT POSITIVE NAND BUFFER

SN74LS37
SN7437

QUADRUPL 2-INPUT
POSITIVE-NAND BUFFERS
37

positive logic:
 $Y = AB$



NOT USED

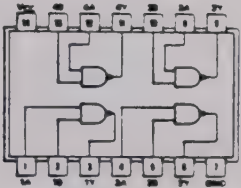
SN5437 (J, W) SN7437 (J, N)
SN54LS37 (J, W) SN74LS37 (J, N)
SN54S37 (J, W) SN74S37 (J, N)

TTL QUADRUPL 2-INPUT POSITIVE NAND BUFFER

SN74LS38
SN7438

QUADRUPL 2-INPUT
POSITIVE-NAND BUFFERS
WITH OPEN-COLLECTOR OUTPUTS
38

positive logic:
 $Y = AB$



665-00155

SN5438 (J, W) SN7438 (J, N)
SN54LS38 (J, W) SN74LS38 (J, N)
SN54S38 (J, W) SN74S38 (J, N)

TTL BCD-TO-DECIMAL DECODER

SN7442

665-00089

- All Outputs Are High for Invalid Input Conditions
- Also for Application as
4-Line-to-16-Line Decoders
3-Line-to-8-Line Decoders
- Diode-Clamped Inputs

TYPES	TYPICAL POWER DISSIPATION	TYPICAL PROPAGATION DELAYS
'42A, '43A, '44A	140 mW	17 ns
'42, '43, '44	70 mW	40 ns
'LS42	36 mW	17 ns

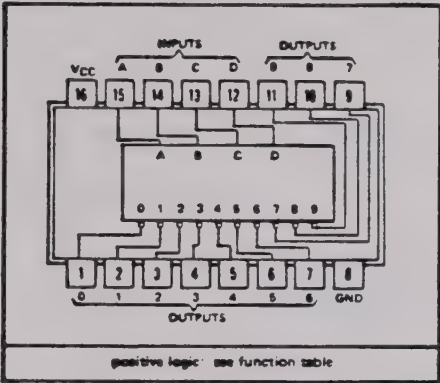
description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The '42A, 'L42, and 'LS42 BCD-to-decimal decoders, the '43A and 'L43 excess-3-to-decimal decoders, and the '44A and 'L44 excess-3-gray-to-decimal decoders feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits. D-c noise margins are typically one volt.

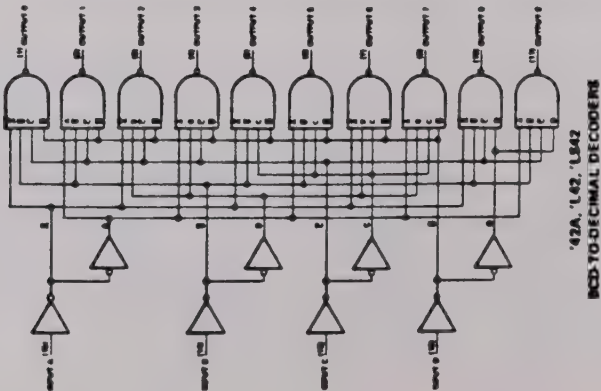
Series 54, 54L, and 54LS circuits are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74, 74L, and 74LS circuits are characterized for operation from 0°C to 70°C.

SN5442A THRU SN5444A, SN54LS42 ... J OR W PACKAGE
SN54L42 THRU SN54L44 ... J PACKAGE
SN7442A THRU SN7444A,
SN74L42 THRU SN74L44, SN74LS42 ... J OR N PACKAGE
(TOP VIEW)



NO.	'42A, 'L42, 'LS42 BCD INPUT				'43A, 'L43 EXCESS-3-INPUT				'44A, 'L44 EXCESS-3-GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
	D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	L	H	L	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H
2	L	L	H	L	L	H	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H
3	L	L	H	H	L	H	H	L	L	H	L	H	H	H	L	H	H	H	H	H	H	H
4	L	H	L	L	L	H	H	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	L	L	L	H	H	H	L	L	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	L	L	H	H	H	L	H	H	H	H	H	H	L	H	H	H	H
7	L	H	H	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H
8	H	L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	L	H	H
9	H	L	L	H	H	H	L	L	H	L	H	L	H	H	H	H	H	H	H	H	L	H
INVALID	H	L	H	L	H	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H

H = high level; L = low level



TTL AND-GATED J-K MASTER-SLAVE FLIP-FLOP WITH PRESET AND CLEAR

SN74LS72
SN7472

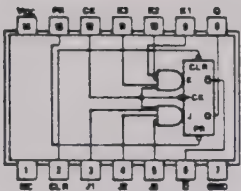
AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

NOT USED

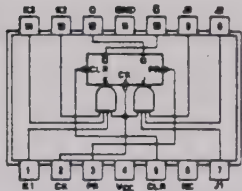
72

FUNCTION TABLE					
INPUTS					OUTPUTS
PRESET	CLEAR	CLOCK	J	K	Q Q̄
L	H	X	X	X	H L
H	L	X	X	X	L H
L	L	X	X	X	H* H*
H	H	⌋	L	L	Q ₀ Q̄ ₀
H	H	⌋	H	L	H L
H	H	⌋	L	H	L H
H	H	⌋	H	H	TOGGLE

positive logic: J = J1·J2·J3; K1·K2·K3



SN7472 (J, N)
SN74H72 (J, N)
SN74L72 (J)



SN7472 (W)
SN74H72 (W)
SN74L72 (T)

NC—No internal connection

TTL DUAL J-K FLIP-FLOP WITH CLEAR

SN74LS73
SN7473

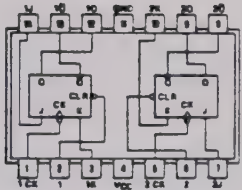
DUAL J-K FLIP-FLOPS WITH CLEAR

NOT USED

73

73, '73, 'L73 FUNCTION TABLE					
INPUTS					OUTPUTS
CLEAR	CLOCK	J	K	Q̄	Q
L	X	X	X	L H	L H
H	⌋	L	L	Q ₀ Q̄ ₀	Q ₀ Q̄ ₀
H	⌋	L	H	L H	L H
H	⌋	H	H	TOGGLE	TOGGLE

'LS73A FUNCTION TABLE					
INPUTS					OUTPUTS
CLEAR	CLOCK	J	K	Q̄	Q
L	X	X	X	L H	L H
H	⌋	L	L	Q ₀ Q̄ ₀	Q ₀ Q̄ ₀
H	⌋	L	H	L H	L H
H	⌋	H	H	TOGGLE	TOGGLE
H	H	X	X	Q ₀ Q̄ ₀	Q ₀ Q̄ ₀



SN7473 (J, N)
SN74H73 (J, N)
SN74L73 (J, N)
SN74LS73A (J, N)

TTL DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESET AND CLEAR

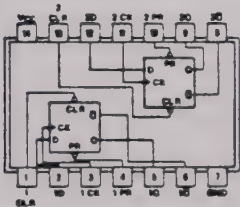
SN74LS74
SN7474

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

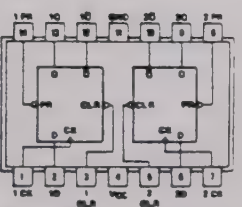
665-00197

74

FUNCTION TABLE					
INPUTS					OUTPUTS
PRESET	CLEAR	CLOCK	D	Q̄	Q
L	H	X	X	H L	H L
H	L	X	X	L H	L H
L	L	X	X	H* H*	H* H*
H	H	⌋	H	L H	L H
H	H	⌋	L	L H	L H
H	H	⌋	X	Q ₀ Q̄ ₀	Q ₀ Q̄ ₀



SN7474 (J, N)
SN74H74 (J, N)
SN74L74 (J, N)
SN74LS74A (J, N)
SN74S74 (J, N)



SN7474 (W)
SN74H74 (W)
SN74L74 (T)

TTL 4-BIT AMPLITUDE COMPARATOR

SN7485N

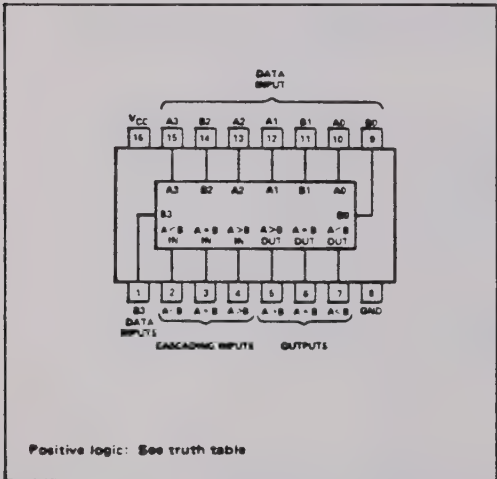
665-00198

DESCRIPTION

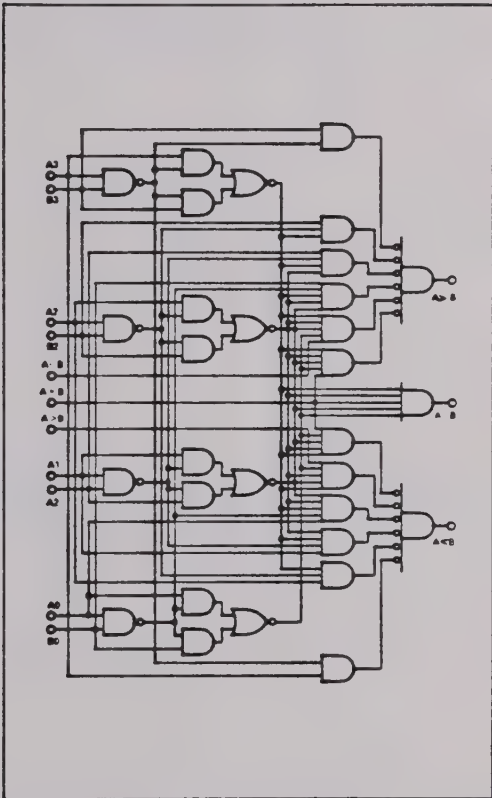
The S5485 and N7485 perform magnitude comparison of straight binary and straight BCD (8421) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. When cascaded, the total time for comparison is the function of the word length; however, only a two-gate-level delay (12 ns) is added for each four-bit expansion.

These circuits are completely compatible with most TTL and DTL families. Typical average power dissipation is 275 milliwatts. The S5485 is characterized for operation over the full military temperature range of -55°C to 125°C; The N7485 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

NOTE: H = High level, L = Low level, X = Irrelevant

TTL QUAD 2-INPUT EXCLUSIVE OR GATE

SN7486N
SN74LS86

665-00189
665-00383

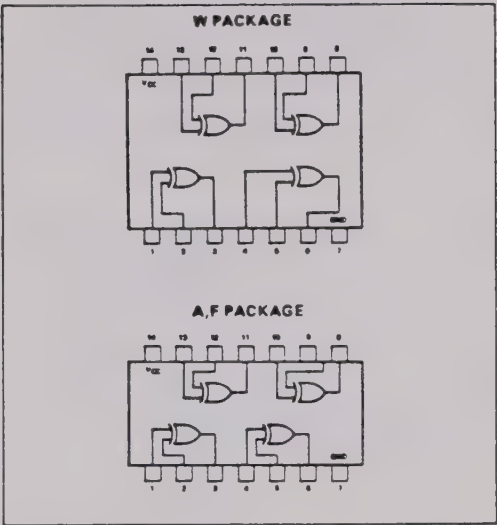
DESCRIPTION

The 54/7486 Quad 2-Input Exclusive OR Gate is a TTL element providing the function $A \oplus B$ at the output.

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}	S5486 Circuits	4.5	5	5.5	V
	N7486 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each output, N :	Logical 0			10	
	Logical 1			20	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	$V_{CC} = \text{MIN}$		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	$V_{CC} = \text{MIN}$				0.8	V
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN}$, $V_{in(1)} = 2V$, $V_{in(0)} = 0.8V$, $I_{load} = -800 \mu A$		2.4			V
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN}$, $V_{in(1)} = 2V$, $V_{in(0)} = 0.8V$, $I_{sink} = 16mA$				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	$V_{CC} = \text{MAX}$, $V_{in} = 2.4V$				40	μA
$I_{in(0)}$	Logical 0 level input current (each input)	$V_{CC} = \text{MAX}$, $V_{in} = 5.5V$				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	$V_{CC} = \text{MAX}$, $V_{in} = 0.4V$				-1.6	mA
I_{OS}	Short circuit output current†	$V_{CC} = \text{MAX}$, $V_{in(1)} = 4.5V$, $V_{in(0)} = 0$		-20		-55	mA
I_{OS}	Short circuit output current†	$V_{CC} = \text{MAX}$, $V_{in(1)} = 4.5V$, $V_{in(0)} = 0$		-18		-55	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, $V_{in} = 4.5V$			30	43	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, $V_{in} = 4.5V$			30	60	mA

TTL DECADA COUNTER

SN7490

665-00076

description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A, 'L90, and 'LS90, divide-by-six for the '92A and 'LS92, and divide-by-eight for the '93A, 'L93, and 'LS93.

All of these counters have a gated zero reset and the '90A, 'L90, and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A, 'L90, or 'LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A .

'90A, 'L90, 'LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	M
2	L	L	M	L
3	L	L	M	M
4	L	M	L	L
5	L	M	L	M
6	L	M	M	L
7	L	M	M	M
8	M	L	L	L
9	M	L	L	M

'90A, 'L90, 'LS90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	M
2	L	L	M	L
3	L	L	M	M
4	L	M	L	L
5	M	L	L	L
6	M	L	L	M
7	M	L	M	L
8	M	L	M	M
9	M	M	L	L

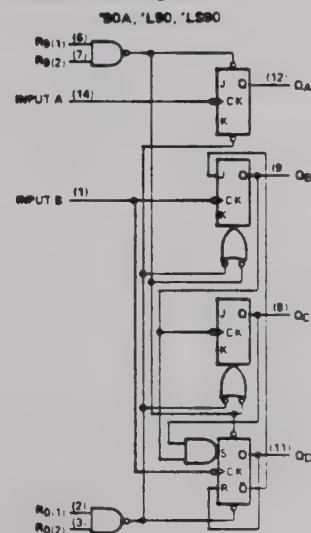
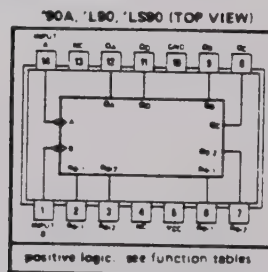
'90A, 'L90, 'LS90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{D(1)}$	$R_{D(2)}$	$R_{B(1)}$	$R_{B(2)}$	Q_D	Q_C	Q_B	Q_A
M	M	L	X	L	L	L	L
M	M	X	L	L	L	L	L
X	X	M	M	M	L	L	M
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

- NOTES A Output Q_A is connected to input B for BCD count
 B Output Q_D is connected to input A for bi-quinary count
 C Output Q_A is connected to input B
 D. H = high level, L = low level, X = irrelevant

functional block diagrams

SN54, SN54LS... J OR W PACKAGE
 SN54L... J OR T PACKAGE
 SN54, SN74L, SN74LS... J OR N PACKAGE



TTL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH CLEAR

SN74LS122
SN74122

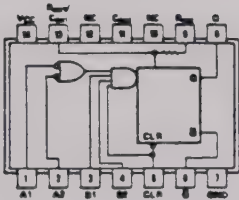
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

NOT USED

122 FUNCTION TABLE

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	X	H	$\uparrow$	$\downarrow$
H	L	X	H	$\uparrow$	$\downarrow$	$\uparrow$
H	X	L	$\uparrow$	H	$\downarrow$	$\uparrow$
H	X	L	H	$\uparrow$	$\downarrow$	$\uparrow$
H	H	X	$\downarrow$	H	$\downarrow$	$\uparrow$
H	X	$\downarrow$	H	H	$\downarrow$	$\uparrow$
H	$\downarrow$	H	H	H	$\downarrow$	$\uparrow$
$\uparrow$	L	X	H	H	$\downarrow$	$\uparrow$
$\downarrow$	X	L	H	H	$\downarrow$	$\uparrow$

- NOTES: 1. An external timing capacitor may be connected between C_{EXT} and R_{EXT}/C_{EXT} (positive).
2. For accurate repeatable pulse widths, connect an external resistor between R_{EXT}/C_{EXT} and V_{CC} with R_{INT} open-circuited.



SN54122 (J, W) SN74122 (J, N)
SN54L122 (J, T) SN74L122 (J, N)
SN54LS122 (J, W) SN74LS122 (J, N)
'122 ... $R_{INT} = 10\text{ k}\Omega$ NOM
'L122 ... $R_{INT} = 20\text{ k}\Omega$ NOM
'LS122 ... $R_{INT} = 10\text{ k}\Omega$ NOM

NC—No internal connection

TTL DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH CLEAR

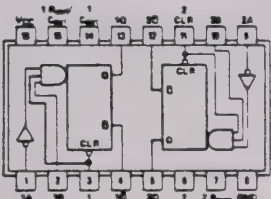
SN74LS123
SN74123

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

665-00139

123 FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	$\uparrow$	$\downarrow$	$\uparrow$
H	$\downarrow$	H	$\downarrow$	$\uparrow$
$\uparrow$	L	H	$\downarrow$	$\uparrow$



SN54123 (J, W) SN74123 (J, N)
SN54L123 (J) SN74L123 (J, N)
SN54LS123 (J, W) SN74LS123 (J, N)

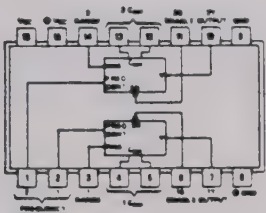
TTL DUAL VOLTAGE-CONTROLLED OSCILLATOR

SN74LS124
SN74124

DUAL VOLTAGE-CONTROLLED OSCILLATORS

NOT USED

124



SN54LS124 (J, W) SN74LS124 (J, N)
SN54S124 (J, W) SN74S124 (J, N)

NC—No internal connection

TTL 3 LINE TO 8 LINE DECODER/DEMULTIPLEXER

- SN74LS138 • Designed Specifically for High-Speed:
Memory Decoders
Data Transmission Systems
- 'S138 and 'LS138 3-to-8-Line Decoders Incorporate 3 Enable Inputs to Simplify Cascading and/or Data Reception
 - 'S139 and 'LS139 Contain Two Fully Independent 2-to-4-Line Decoders/ Demultiplexers
 - Schottky Clamped for High Performance

TYPE	TYPICAL PROPAGATION DELAY (3 LEVELS OF LOGIC)	TYPICAL POWER DISSIPATION
'LS138	22 ns	32 mW
'S138	8 ns	245 mW
'LS139	22 ns	34 mW
'S139	7.5 ns	300 mW

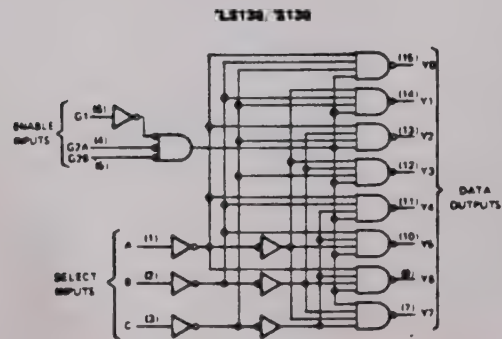
description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

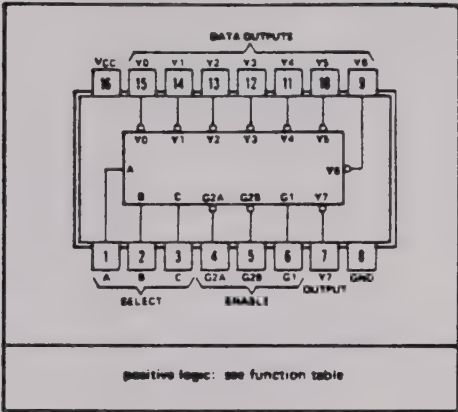
The 'LS138 and 'S138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The 'LS139 and 'S139 comprise two individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs each of which represents only one normalized Series 54LS/74LS load ('LS138, 'LS139) or one normalized Series 54S/74S load ('S138, 'S139) to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design. Series 54LS and 54S devices are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74LS and 74S devices are characterized for 0°C to 70°C industrial systems.



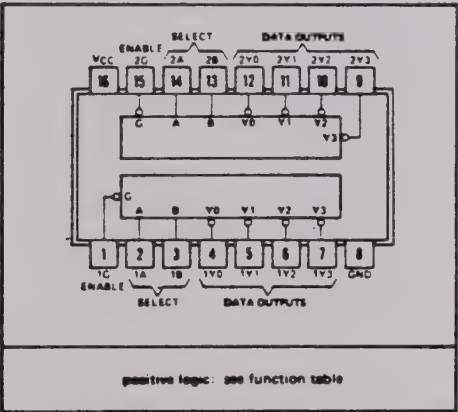
SN54LS138, SN54S138 ... J OR W PACKAGE
SN74LS138, SN74S138 ... J OR N PACKAGE
(TOP VIEW)



665-00140

NOT USED

SN54LS139, SN54S139 ... J OR W PACKAGE
SN74LS139, SN74S139 ... J OR N PACKAGE
(TOP VIEW)



NOT USED

'LS138, 'S138
FUNCTION TABLE

INPUTS		OUTPUTS							
ENABLE	SELECT								
G1 G2*	C B A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X H	X X X	H	H	H	H	H	H	H	H
L X	X X X	X	X	X	X	X	X	X	X
H L	L L L	L	H	H	H	H	H	H	H
H L	L L H	H	L	H	H	H	H	H	H
H L	L H L	H	H	L	H	H	H	H	H
H L	L H H	H	H	H	L	H	H	H	H
H L	H L L	H	H	H	H	L	H	H	H
H L	H L H	H	H	H	H	H	L	H	H
H L	H H L	H	H	H	H	H	H	L	H
H L	H H H	H	H	H	H	H	H	H	L

*G2 = G2A • G2B
H = high level, L = low level, X = irrelevant

NOT USED

BCD-TO-DECIMAL DECODER DRIVER

SN74145

665-00369

FOR USE AS LAMP, RELAY, OR MOS DRIVERS

- Full Decoding of Input Logic
- SN54145, SN74145, and SN74LS145 Have 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions
- Low Power Dissipation of 'LS145... 35 mW Typical

logic

FUNCTION TABLE

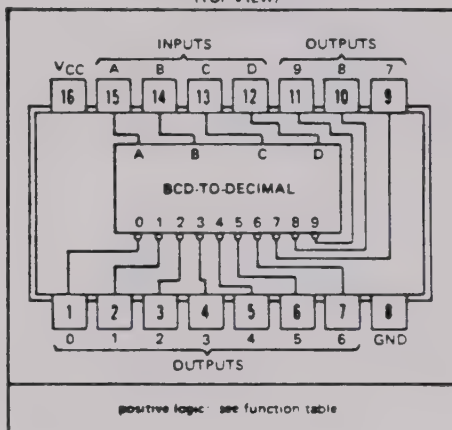
NO	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H

H = high level (off), L = low level (on)

description

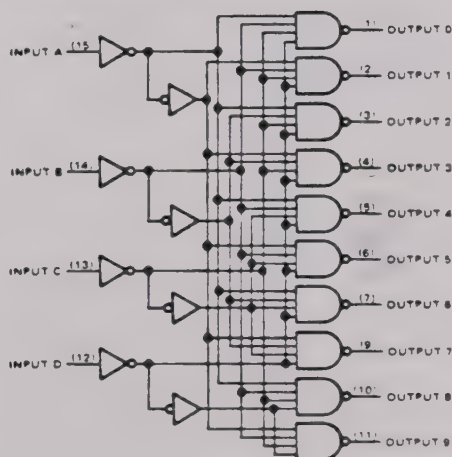
These monolithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (15 volts) of the SN54145, SN74145, or SN74LS145 will sink up to 80 milliamperes of current. Each input is one Series 54/74 or Series 54LS/74LS standard load, respectively. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts for the '145 and 35 milliwatts for the 'LS145.

SN54145, SN54LS145... J OR W PACKAGE
SN74145, SN74LS145... J OR N PACKAGE
(TOP VIEW)



positive logic - see function table

functional block diagram



TTL DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

SN74LS153

665-00080

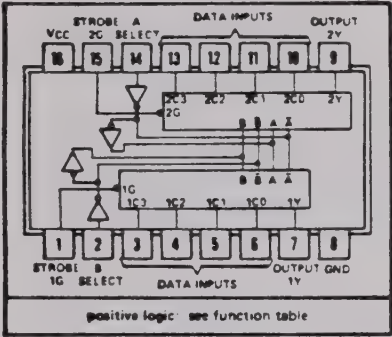
- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with most TTL and DTL Circuits

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIMES			TYPICAL POWER DISSIPATION
	FROM DATA	FROM STROBE	FROM SELECT	
'153	14 ns	17 ns	22 ns	180 mW
'L153	27 ns	34 ns	44 ns	90 mW
'LS153	14 ns	19 ns	22 ns	31 mW
'S153	6 ns	9.5 ns	12 ns	225 mW

description

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

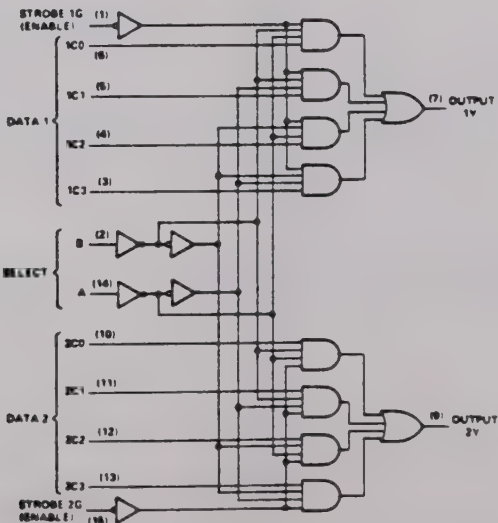
SN74153, SN74L153, SN74LS153, SN74S153 ... J OR N PACKAGE
(TOP VIEW)



SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections
H = high level, L = low level, X = irrelevant

functional block diagram



TTL QUAD 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

665-00339

SN74LS157

features

- Buffered Inputs and Outputs
- Three Speed/Power Ranges Available

TYPES	TYPICAL AVERAGE PROPAGATION TIME	TYPICAL POWER DISSIPATION
'157	9 ns	150 mW
'L157	18 ns	75 mW
'LS157	9 ns	40 mW
'S157	5 ns	250 mW
'LS158	7 ns	24 mW
'S158	4 ns	195 mW

applications

- Expand Any Data Input Point
- Multiplex Dual Data Buses
- Generate Four Functions of Two Variables (One Variable Is Common)
- Source Programmable Counters

description

These monolithic data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The '157, 'L157, 'LS157, and 'S157 present true data whereas the 'LS158 and 'S158 present inverted data to minimize propagation delay time.

FUNCTION TABLE

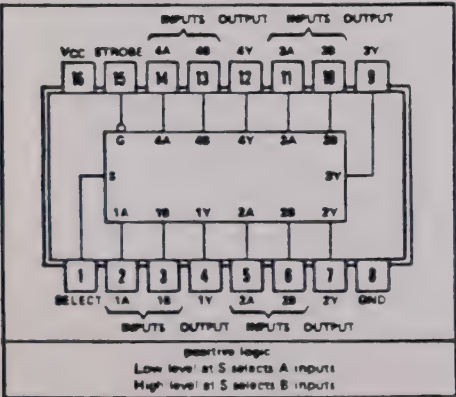
INPUTS				OUTPUT Y	
STROBE	SELECT	A	B	'157, 'L157, 'LS157, 'S157	'LS158 'S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant

SN54157, SN54LS157, SN54S157 ... J OR W PACKAGE

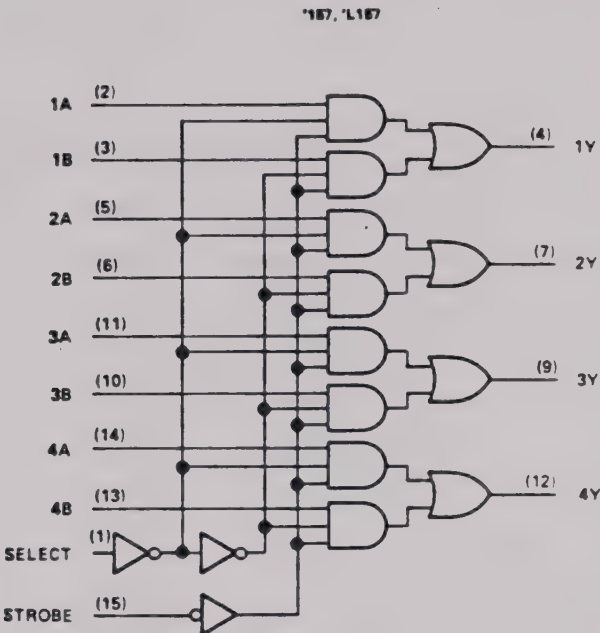
SN54L157 ... J PACKAGE

SN74157, SN74LS157, SN74S157 ... J OR N PACKAGE
(TOP VIEW)

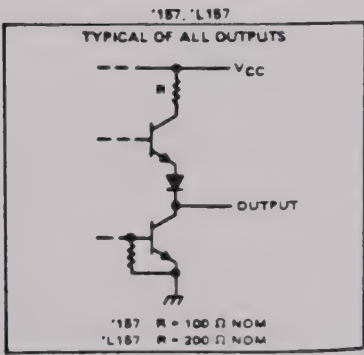
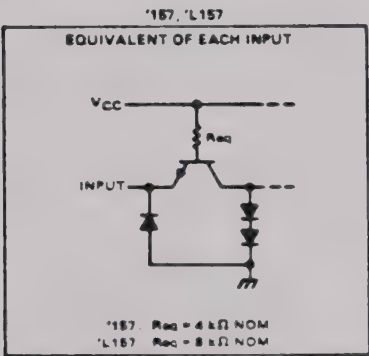


positive logic
Low level at S selects A inputs
High level at S selects B inputs

functional block diagram



schematics of inputs and outputs



TTL HEX/QUAD D TYPE FLIP-FLOP

SN74LS174
SN74LS175

665-00153

'174, 'LS174, 'S174... HEX D-TYPE FLIP-FLOPS
'175, 'LS175, 'S175... QUADRUPLE D-TYPE FLIP-FLOPS

- '174, 'LS174, 'S174 Contain Six Flip-Flops with Single-Rail Outputs
- '175, 'LS175, 'S175 Contain Four Flip-Flops with Double-Rail Outputs
- Three Performance Ranges Offered: See Table Lower Right
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and 'S175 feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

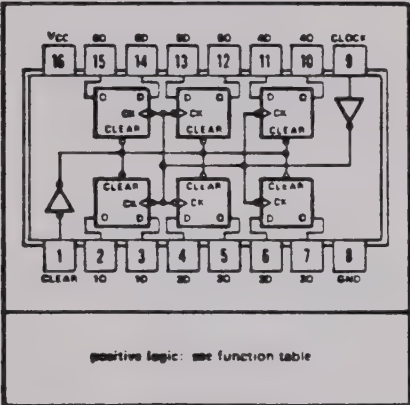
These circuits are fully compatible for use with most TTL or DTL circuits.

FUNCTION TABLE
(EACH FLIP-FLOP)

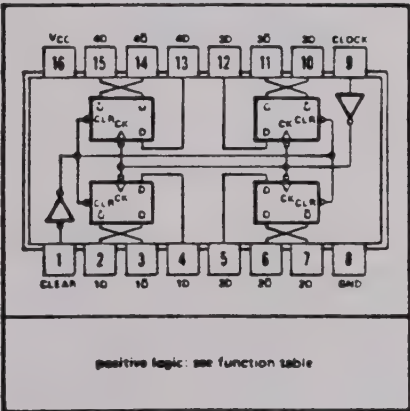
INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
 Q_0 = the level of Q before the indicated steady-state input conditions were established
↑ = '175, 'LS175, and 'S175 only

SN54174, SN54LS174, SN54S174... J OR W PACKAGE
SN74174, SN74LS174, SN74S174... J OR N PACKAGE
(TOP VIEW)



SN54175, SN54LS175, SN54S175... J OR W PACKAGE
SN74175, SN74LS175, SN74S175... J OR N PACKAGE
(TOP VIEW)



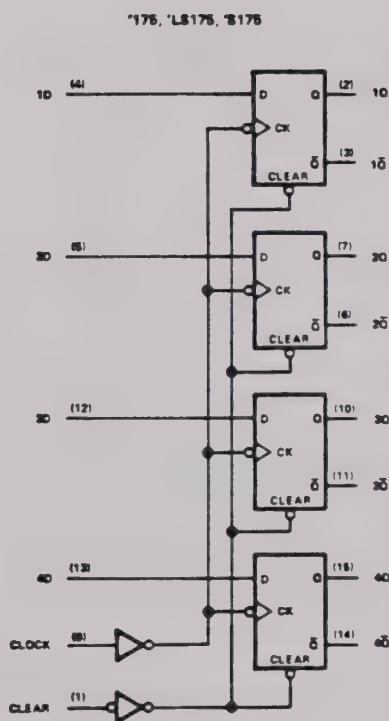
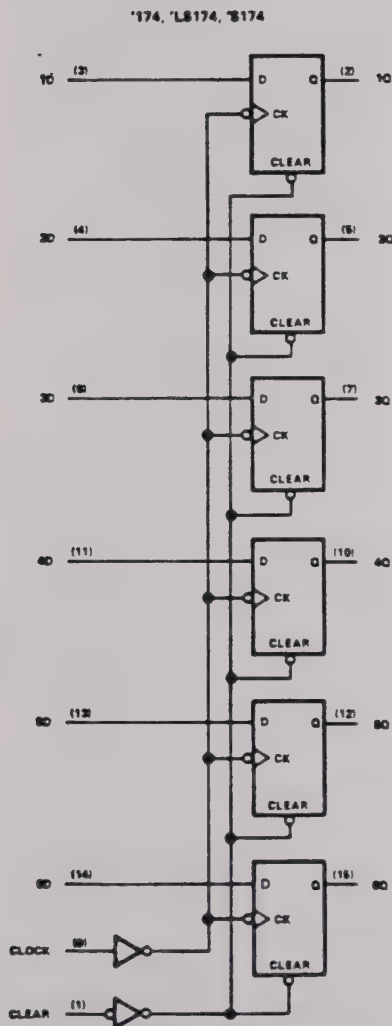
TYPES	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'174, '175	35 MHz	38 mW
'LS174, 'LS175	40 MHz	14 mW
'S174, 'S175	110 MHz	75 mW

TTL HEX/QUAD D TYPE FLIP-FLOP (Cont'd)

SN74LS174
SN74LS175
SN74175

665-00341
665-00183

functional block diagrams



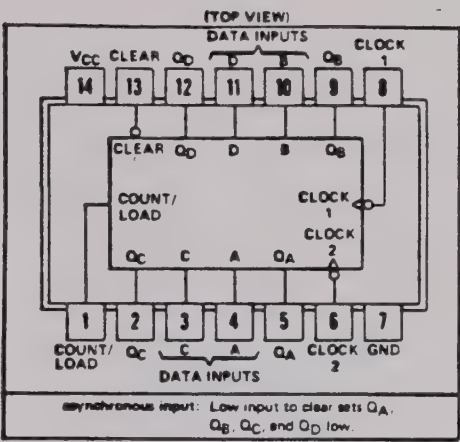
0-50 & 0-25 MHZ PRESETTABLE DECADE COUNTER/LATCH

SN74196N
SN74175

665-00341
665-00183

- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Input Clamping Diodes Simplify System Design
- Output QA Maintains Full Fan-out Capability In Addition to Driving Clock-2 Input

TYPES	GUARANTEED		TYPICAL
	COUNT	FREQUENCY	
	CLOCK 1	CLOCK 2	POWER DISSIPATION
'196, '197	0-50 MHz	0-25 MHz	340 mW
'LS196, 'LS197	0-30 MHz	0-15 MHz	80 mW
'S196, 'S197	0-100 MHz	0-50 MHz	375 mW



description

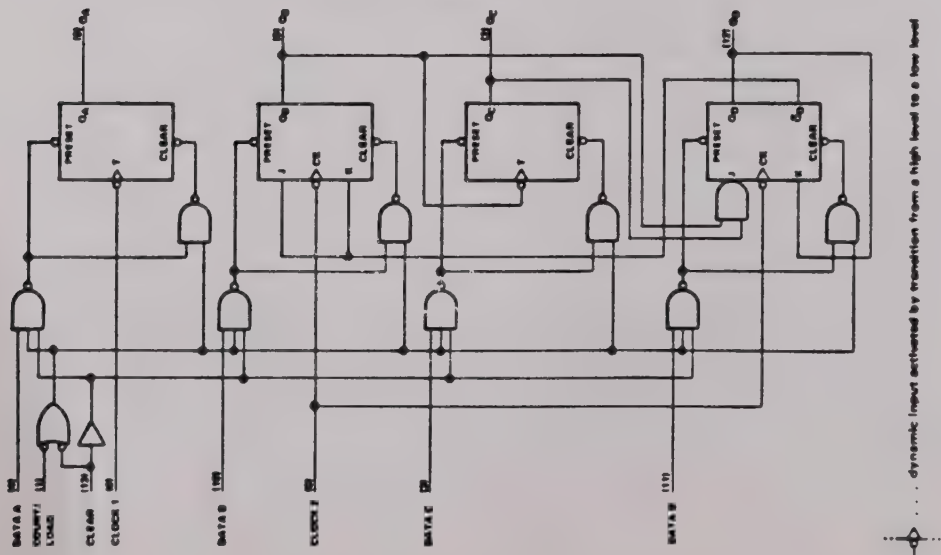
These high-speed monolithic counters consist of four d-c coupled, master-slave flip-flops, which are internally interconnected to provide either a divide-by-two and a divide-by-five counter ('196, 'LS196, 'S196) or a divide-by-two and a divide-by-eight counter ('197, 'LS197, 'S197). These four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. These circuits are compatible with most TTL and DTL logic families. Series 54, 54LS, and 54S circuits are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74, 74LS, and 74S circuits are characterized for operation from 0°C to 70°C.

functional block



DUAL PERIPHERAL DRIVERS

SN75452P NAND DRIVER
SN75453P OR DRIVER

665-00077

DUAL PERIPHERAL DRIVERS

These versatile devices are useful for interfacing digital logic to industrial electronic systems. They are useful as lamp drivers, relay drivers, logic buffers, line drivers, or MOS drivers.

Each of these devices consists of a pair of MTTL gates with the output of each gate internally connected to the base of a transistor.

MC75451 provides the AND function
MC75452 provides the NAND function
MC75453 provides the OR function
MC75454 provides the NOR function

- 300 mA Output Current Capability
- Output Breakdown Voltage - 30 V Min
- MTTL compatible Inputs

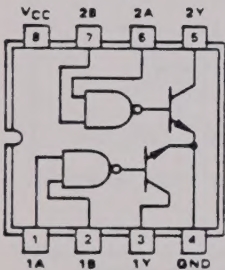


U SUFFIX
CERAMIC PACKAGE
CASE 693



P SUFFIX
PLASTIC PACKAGE
CASE 626

MC75451 - Positive AND



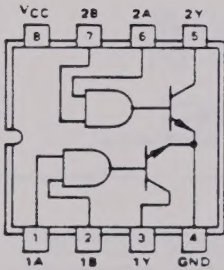
Positive Logic $Y = AB$

TRUTH TABLE

A	B	Y
L	L	L (ON state)
L	H	L (ON state)
H	L	L (ON state)
H	H	H (OFF state)

H = high level; L = low level

MC75452 - Positive NAND



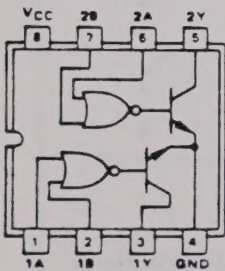
Positive Logic $Y = \overline{AB}$

TRUTH TABLE

A	B	Y
L	L	H (OFF state)
L	H	H (OFF state)
H	L	H (OFF state)
H	H	L (ON state)

H = high level; L = low level

MC75453 - Positive OR



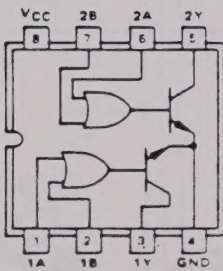
Positive Logic $Y = A + B$

TRUTH TABLE

A	B	Y
L	L	L (ON state)
L	H	H (OFF state)
H	L	H (OFF state)
H	H	H (OFF state)

H = high level; L = low level

MC75454 - Positive NOR



Positive Logic $Y = \overline{A + B}$

TRUTH TABLE

A	B	Y
L	L	H (OFF state)
L	H	L (ON state)
H	L	L (ON state)
H	H	L (ON state)

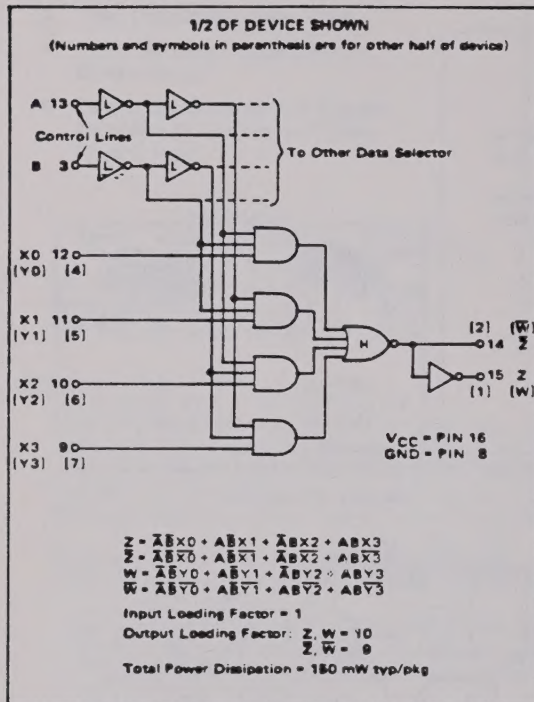
H = high level; L = low level

TTL DUAL 4-INPUT MULTIPLEXER, COMPLEMENTARY OUTPUT

MC8309P

665-00133

665-00100



This device consists of two four-channel data selectors with common control lines, constructed from high-level AND-OR-INVERT gates with active pullup outputs, and low-level inverters on the control inputs. By selecting one of four logic combinations, information on one of the four data inputs will be routed to the complementary outputs.

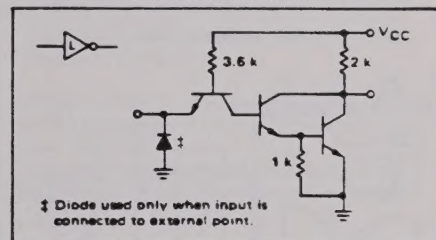
Data selectors are useful in applications where digital data is to be routed from one of several registers or locations to another register or location for processing.

The MC9309/8309 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output buss.

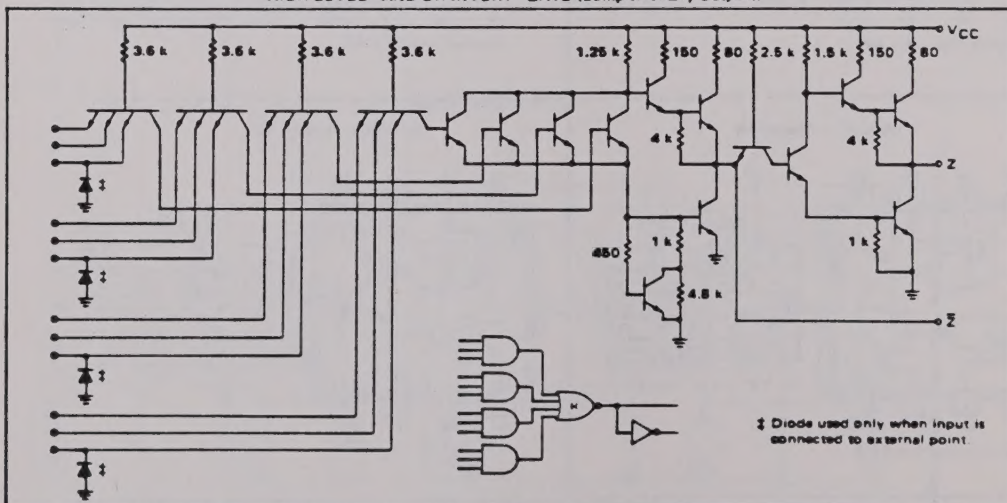
TYPICAL PROPAGATION DELAY TIMES (ns)
 $T_A = 25^\circ\text{C}$

INPUT	Z	$\bar{Z}$	CONDITIONS
A	24	16	X0 = X2 = X3 = logic "0", X1 = logic "1". A and B are defined by the logic equations
X1	17	9	

LOW-LEVEL INVERTER



HIGH-LEVEL "AND-OR-INVERT" GATE (Complementary Outputs)



* L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

MP MASTER



MA33937